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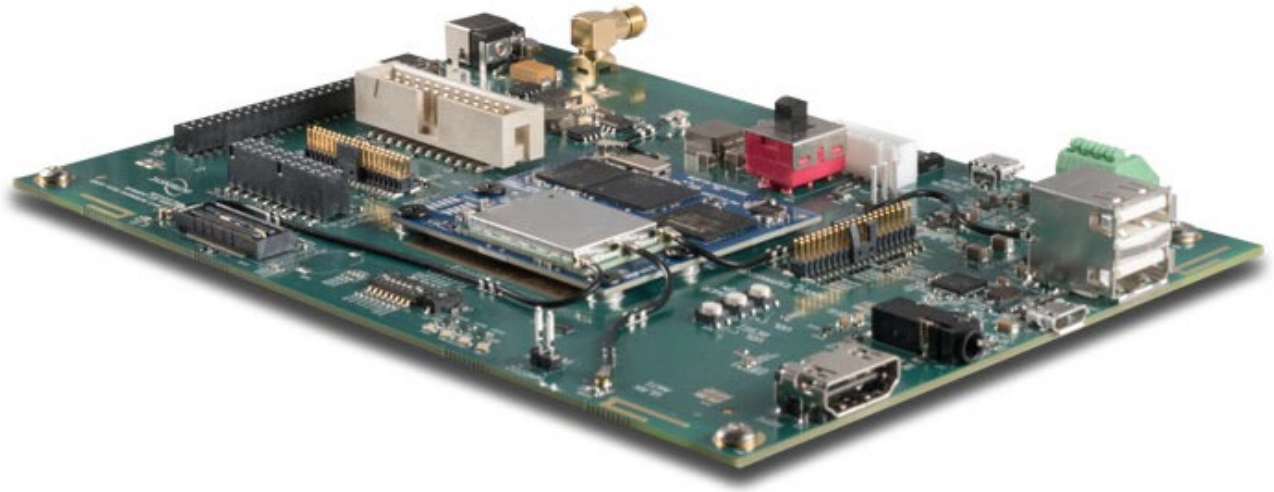

Open-Q™ 624A Development Kit User Guide

Part Number PMD-00065

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Revision History

Date	Rev.	Comments
January 2018	1.0	Initial release. Intrinsyc document number: ITC-01RND1397-UG-001
March 2019	1.1	• Added section 3.5. • Added block diagram of GNSS front end • Added commands to configure display output • Updated photos
August 2020	A	Initial Lantronix document. Added Lantronix document part number, Lantronix logo, branding, contact information, and links.

For the latest revision of this product document, please go to: http://tech.intrinsyc.com.

Contents

1 Introduction

1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q™ 624A Development Kit

For more background information on this development kit, visit: https://www.intrinsyc.com/snapdragon-embedded-development-kits/open-q-624a-development-kit/

1.2 Scope

This document will cover the following items on the Open-Q 624A:

- Block Diagram and Overview
- Hardware Features
- Configuration
- SOM
- Carrier Board
- Accessories

1.3 Intended Audience

This document is intended for users of the Lantronix Open-Q 624A Development Kit.

2 Documents

This section lists the supplementary documents for the Open-Q 624A development kit.

2.1 Applicable Documents

Reference	Title
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.2 Reference Documents

Documents available on the Lantronix support portal for registered customers.

Reference	Title
R-1	Open-Q™ 624A Schematics (SOM, Carrier)
R-2	Open-Q™ 624A SOM Tech Note 48 (Carrier Board Design Guide)
R-3	Open-Q™ 624A SOM Device Specification

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission

Term and acronyms	Definition
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SOM	System on Module
SPMI	System Power Management Interface (Qualcomm PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

2.4 List of Figures

2.5 List of Tables

3 Open-Q™ 624A Development Kit

3.1 Introduction

The Open-Q 624A Development Kit provides an evaluation platform for the Qualcomm 624 processor and the Open-Q 624A SOM. This kit is suited for Android / Linux application developers, OEMs, consumer manufacturers, hardware component vendors, to evaluate, optimize, test and deploy applications that can utilize the Qualcomm 624 chipset.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 624A Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

3.4 Kit Contents

The Open-Q 624A Development Kit includes the following:

- Open-Q™ 624A SOM with the Qualcomm 624 (APQ8053-Lite) processor
- Open-Q™ 624A Carrier board
- AC power adapter
- HDMI cable

- LCD / Touchscreen (Optional accessory)
- Camera module and adaptor board (Optional accessory)
- Quick Start Guide

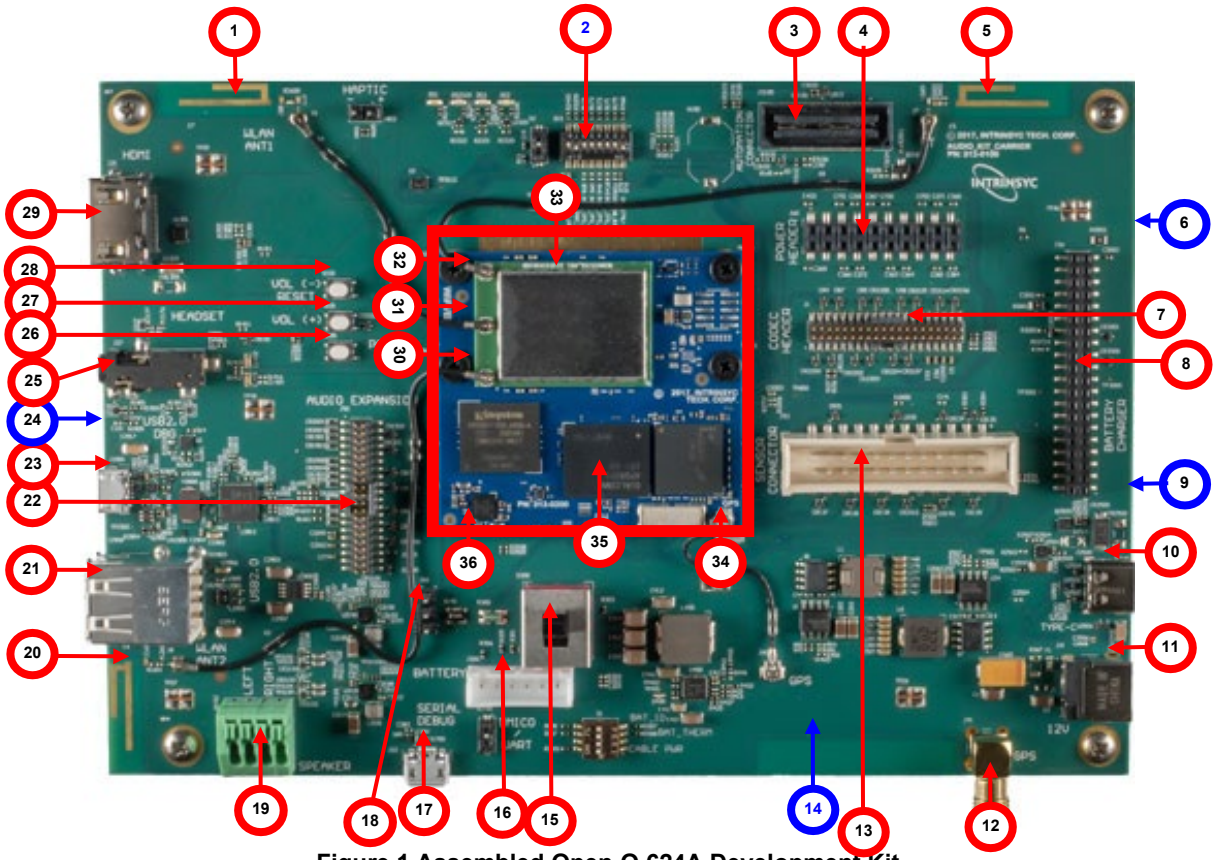

Figure 1 Assembled Open-Q 624A Development Kit

1. WLAN Antenna 1 (PCB Trace)
2. Configuration DIP switches
3. Automation Header
4. Power header
5. BT Antenna (PCB trace)
6. MIPI-CSI Camera 0 Connector*
7. Digital Audio Codec header
8. Battery Charging header
9. MIPI-CSI Camera 1 Connector*
10. USB Type-C Connector
11. 12V DC Power jack
12. GPS External Antenna Connector
13. Sensor header
14. GPS PCB Antenna*
15. Power Source Switch (Batt/DC)
16. Battery connector
17. USB Debug UART Micro B
18. SOM Power Probe header
19. Speaker Connector
20. WLAN Antenna 2 (PCB Trace)
21. USB Type-A (Not supported)
22. Audio Expansion Header
23. Micro-USB port (not supported)
24. MIPI-DSI LCD/Display Connector*
25. Headset Connector
26. Power Button
27. Volume + button
28. Volume - button
29. HDMI Connector
30. Wi-Fi U.FL Antenna 0 Connector
31. Wi-Fi U.FL Antenna 1 Connector
32. BT U.FL Antenna Connector
33. WLAN/BT Module
34. GPS U.FL Antenna Connector
35. Qualcomm APQ8053-Lite CPU
36. Open-Q 624A System on Module (SOM)

* ON BOTTOM SIDE

The development kit comes with Android software pre-programmed on the CPU board (SOM). Please contact Lantronix for availability of display adaptors, camera modules, sensor boards, and other accessories: sales@lantronix.com

3.5 Getting Started

This section explains how to setup the Open-Q 624A Development Kit and start using it.

3.5.1 Registration

To register the development kit and gain access to the Lantronix support site, please visit: https://tech.intrinsyc.com/account/register.

To proceed with registration, the development kit serial number is required. The serial number can be found on the label on the top side of the SOM. The label contains the Serial Number and WIFI MAC address.

Note: Please retain the Development Kit serial number for warranty purposes.

Refer to http://tech.intrinsyc.com/projects/serialnumber/wiki for more details about locating the development kit serial number.

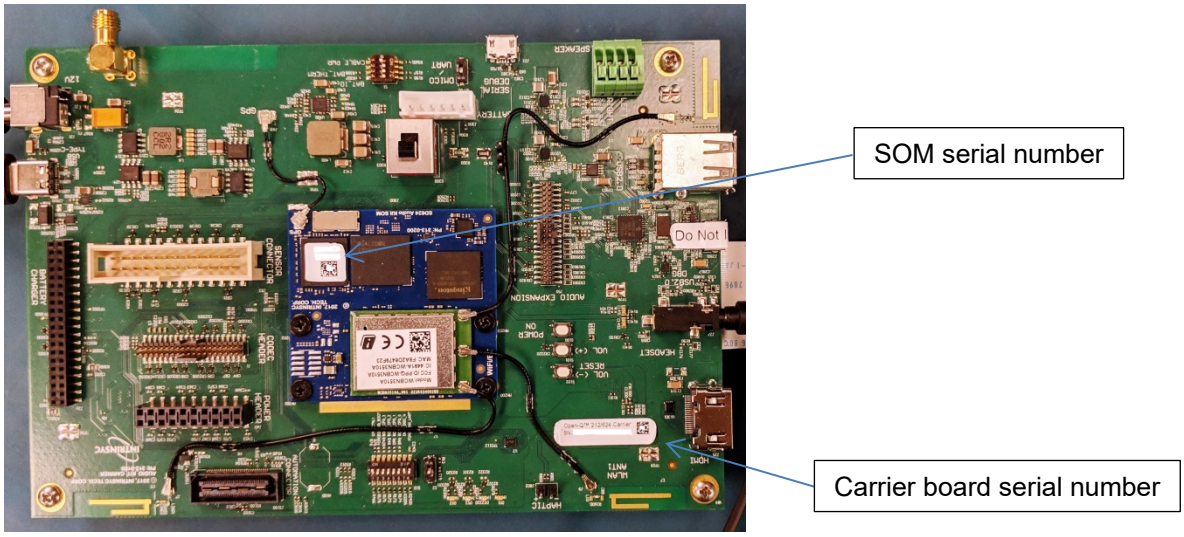

Figure 2: Development Kit label location

3.5.2 HDMI monitor connection

Connect an HDMI monitor to the HDMI output connector (29) with the HDMI cable (unless using the optional LCD/touchscreen)

3.5.3 Powering Up the Development Kit

Connect the Power Adapter to the 12V DC Jack (11) and then press and hold the ON/OFF button (26) until you see the Lantronix logo appear on the display (~3 seconds)

3.6 Development Kit Block Diagram

The block diagram below shows the complete Open-Q 624A development platform, including the SOM and carrier board.

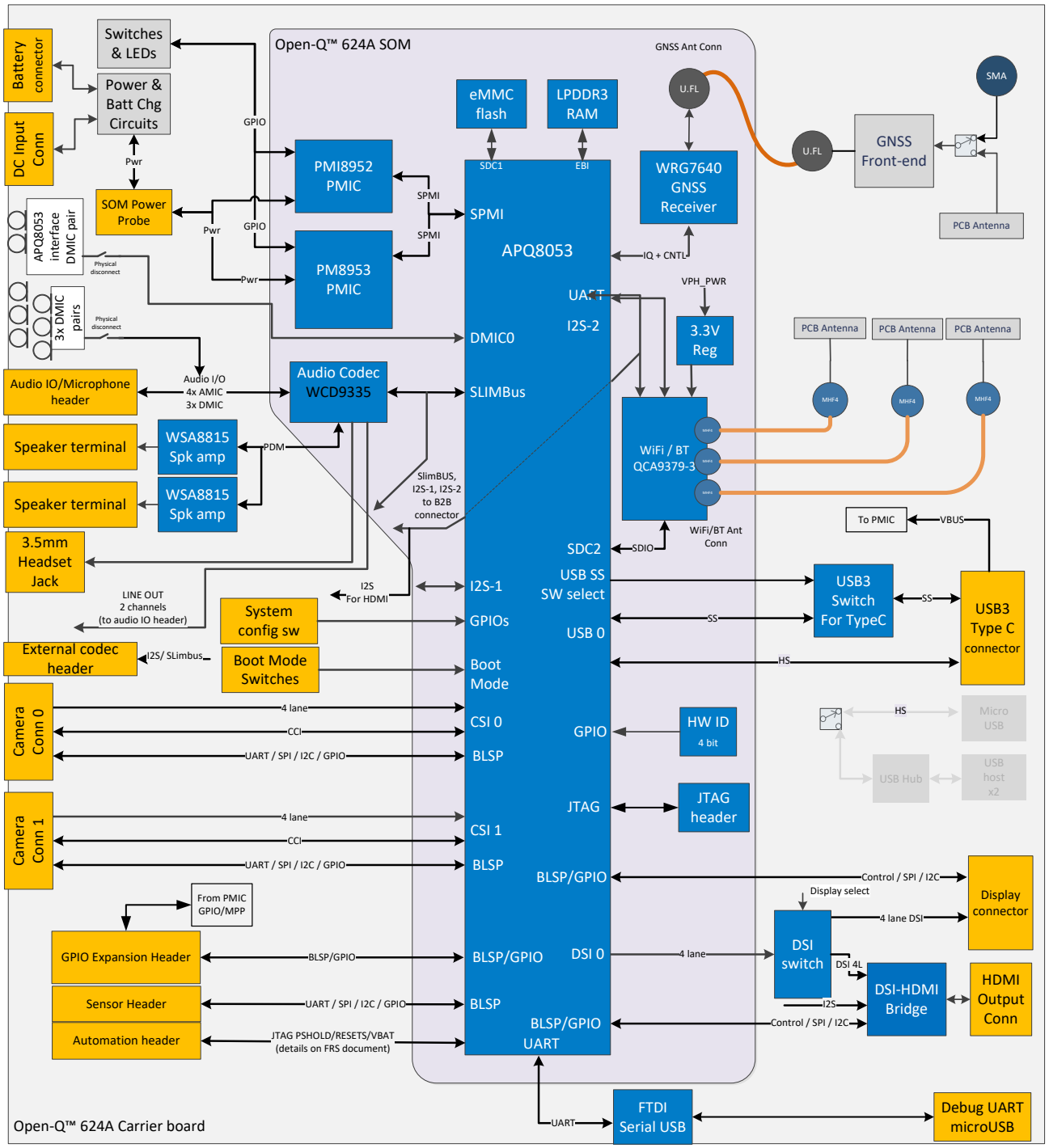

Figure 3 Open-Q 624A Platform Block Diagram

3.7 Open-Q 624A SOM

The Open-Q 624A SOM measures 50mm x 46.5mm and is connected to the carrier board via three 100-pin SOM to carrier board connectors (B2B Connectors). It provides the basic common set of features with minimal integration efforts for end users to design into a product. For more details please refer to the Open-Q™ 624A SOM Device Specification document (R-3).

It contains the following key components:

- Qualcomm 624 (APQ8053-Lite) application processor
- 2GB LPDDR3 RAM, 4GB eMMC Flash
- PMI8952 + PM8953 power management ICs (PMIC) for peripheral LDOs, boost regulators, battery charging, and other house-keeping functions
- Pre-certified 802.11ac 2x2 MU-MIMO Wi-Fi/BT Module with independent Bluetooth antenna port for Bluetooth – Wi-Fi isolation
- Integrated GNSS receiver for GPS, GLONASS, COMPASS location support.

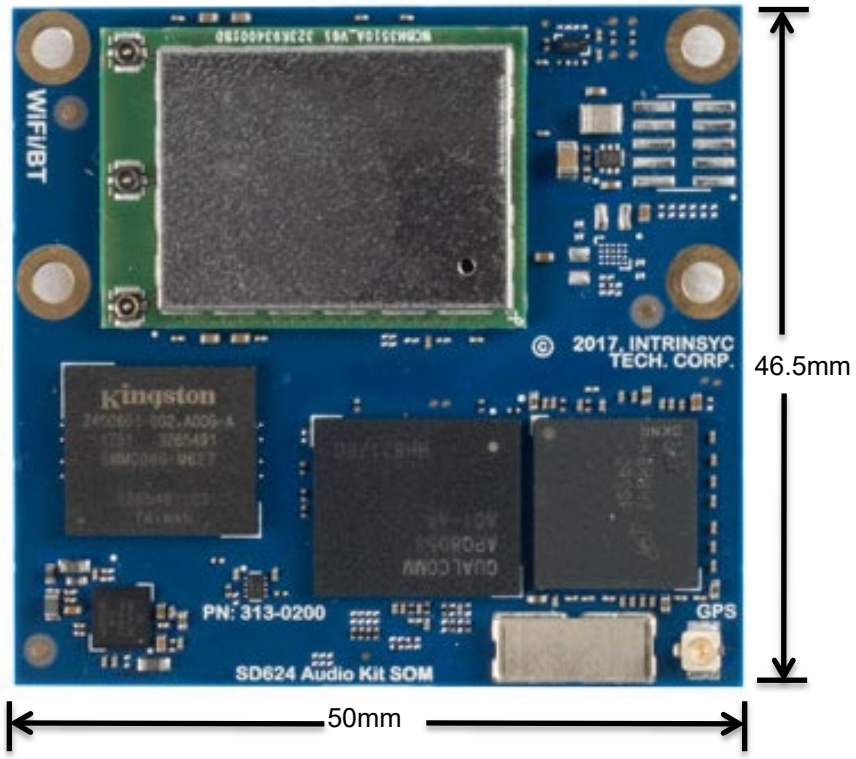

Figure 4 Open-Q 624A SOM

3.7.1 Hardware Features

The Open-Q™ 624A SOM platform includes the following key features:

Table 3-1 Open-Q 624A SOM Features

Feature	Specification
Processor	Qualcomm® 624 (APQ8053-Lite) built on 14nm technology Octa-Core 64-bit ARM Cortex A53 1.8GHz Qualcomm Adreno™ 506 GPU OpenGL ES 3.1, OpenCL 2.0 Full, DirectX 12, GPU Tessellation, Geometry Shading Qualcomm Hexagon™ 546 DSP
Power Management	PMIC (PM8953 & PMi8952) Qualcomm® PMICs. Supports Qualcomm® Quick Charge™ 2.0 and 3.0 technology for fast charging.
Memory/Storage	2GB LPDDR3 RAM, 4GB eMMC Flash
Wireless Connectivity	Wi-Fi/BT module - 802.11a/b/g/n/ac, 2x2 MU-MIMO, 2.4/5Ghz, Bluetooth 4.2 + BLE, using Qualcomm QCA9379-3 3x MHF4 antenna connectors - 2 for Wi-Fi, 1 separate for Bluetooth
GNSS Receiver	Qualcomm WGR7640 - GPS/ GLONASS/ COMPASS U.FL antenna connector with 2.7v bias for active antenna
LCD/Touchscreen Interface	1x 4-lane MIPI DSI LCD up to 1080P Full HD 60fps
Camera Interface	Up to 21MP with 2x 4-lane MIPI CSI and dual ISPs
Video	Video Capture up to 4K Ultra HD at 30fps Video Playback 4K Ultra HD H.264 (AVC) and H.265 (HEVC)
Audio Interfaces	I2S & SlimBus interfaces for external audio devices 2x digital mic inputs directly to processor Qualcomm WCD9335 Audio Codec (4 Analog Inputs, 4 MIC Bias outputs, Headphone output, Stereo Line-Out, 3 digital mic inputs supporting 6 digital mics)
I/O	1x USB3.0 Type-C, multiple BLSP ports (GPIO, UART, SPI, I2C buses), debug UART
OS Support	Android
Operating Environment	Power input: 3.6V to 4.2V Operating Temperature: 0°C to +50°C Carrier board connection: 3x 100 pin board-to-board connectors Size: 50mm x 46.5mm

3.7.2 SOM RF Interfaces for Wi-Fi and Bluetooth Antennas

The Wi-Fi/BT module on the SOM includes the following RF antenna interfaces:

- ANT0: Wi-Fi antenna 1
- ANT1: Wi-Fi antenna 2
- ANT2: Bluetooth antenna

Wi-Fi antennas: The ANT0 port is for one of the two Wi-Fi antennas and ANT1 is for the other Wi-Fi antenna. Since the Wi-Fi module uses 2x2 MIMO technology and operates in both the 2.4GHz and 5GHz bands, two dual-band antennas are required to be connected to achieve the full performance of the Wi-Fi interface. By default, both antenna ports are connected to the carrier board PCB antennas labelled “WLAN ANT1” and “WLAN ANT2” via coaxial cables. Other suitable antennas may be used by connecting them directly to the Wi-Fi antenna ports on the module with MHF4 coaxial connectors.

Bluetooth antenna: The ANT2 port is for a dedicated Bluetooth antenna. By default, this port is connected to the carrier board PCB antenna labelled “BT” via a coaxial cable.

The Wi-Fi/BT module is designed with a dedicated Bluetooth antenna port so that the Bluetooth and Wi-Fi antennas can be physically separated in the end product to provide better isolation between them. This is done to improve concurrent Wi-Fi and Bluetooth operation. The greater the separation between antennas, the better the concurrent Wi-Fi – Bluetooth performance will be.

For details on how the Wi-Fi module connects to the on-board PCB antennas on the carrier board, refer to section 0.

3.7.3 SOM RF Interface for GNSS Antenna

The SOM includes one U.FL type coaxial connector for the GNSS receiver antenna, with a +2.7v bias on it to provide power for an active GNSS antenna. By default, this port is connected to the carrier board PCB antenna labelled “GPS” via a coaxial cable. If desired, a suitable GNSS antenna with a U.FL connector could be connected directly to the SOM antenna port by carefully removing the carrier board coaxial cable.

For more information about connecting a GPS antenna to the development kit see section 3.8.18 below.

3.8 Open-Q™ 624A Carrier Board

The Open-Q 624A Carrier board measures 17cm x 11.5cm (195.5cm^2), and has various connectors used for connecting different peripherals.

Table 3-2 Open-Q 624A Carrier Board Features

Feature	Specification	
LCD/Touchscreen interface	1x 4-lane MIPI DSI connector for optional LCD/touchscreen LCD up to 1080p full HD 60fps	
Camera	2x 4-lane MIPI CSI camera connectors	
Video	Video Capture up to 4K Ultra HD at 30fps Video Playback 4K Ultra HD H.264 (AVC) and H.265 (HEVC) HDMI Type A, 1080p at 60fps	
Audio	Carrier Board Audio Features: ▪ 2 Qualcomm speaker amps (WSA8815) ▪ Stereo speaker terminals ▪ 1x 3.5 mm headset interface ▪ 8x digital microphones on carrier board	Audio Expansion: ▪ Analog and digital audio expansion headers: ▫ 4x analog microphone inputs ▫ 8x digital mic inputs ▫ 1x stereo line output ▪ I2S/SLIMBUS interface for external audio devices
I/O	1x USB3.0 Type C, debug UART USB interface, GPIO expansion header (GPIO, UART, SPI, I2C buses), Haptic output, Sensor Expansion header	
Wireless antennas	2x dual-band (2.4GHz + 5GHz) Wi-Fi PCB antennas Separate Bluetooth PCB antenna for isolation	
GPS	RF Front End (LNA + SAW filter), option to use on-board PCB antenna or connect external SMA antenna +2.7V bias provided on external antenna port for powering an active antenna	
OS support	Android	
Operating environment	▪ Power input: 12V/3A or single-cell Li-ion battery ▪ SOM size: 50mm x 46.5mm ▪ Carrier board size: 170mm x 115mm	

3.8.1 Open-Q™ 624A Carrier Board Expansion Connectors

The following sections will provide in depth information on each expansion header and connector on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-Q™ 624A. Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the processor.

3.8.2 Dip switch S10 Configuration Options

There is a DIP switch S10 on the top side of the Open-Q™ 624A carrier board. The 8-bit switch allows the user to control the system configuration and boot options. Table 3-3 below outlines the pin outs and connections of these DIP switches.

Table 3-3 Dip Switch HW / SW configuration

Function	DIP Switch	Description	Notes
GPS_CTRL1	S10-1	Configures GPS antenna from external SMA connector to onboard PCB antenna.	Default out of the box configuration is OFF, or PCB antenna selected.
FORCED_USB_BOOT	S10-2	Enables FORCE USB (GPIO 37) when DIP switch turned on	Default out of the box configuration is OFF **Note:** FORCE USB boot option not supported by Lantronixc
BOOT_CONFIG[3]	S10-3	Enables APQ boot configuration 3 when DIP switch turned on. Controlled by APQ GPIO109 See schematic for boot configuration options. NOTE: Some boot configurations are not supported on the development kit.	Default out of the box configuration is OFF
BOOT_CONFIG[2]	S10-4	Enables APQ boot configuration 2 when DIP switch turned on. Controlled by APQ-GPIO107	Default out of the box configuration is OFF
BOOT_CONFIG[1]	S10-5	Enables APQ boot configuration 1 when DIP switch turned on. Controlled by APQ-GPIO 113	Default out of the box configuration is OFF
BOOT_CONFIG[0]	S10-6	Enables APQ boot configuration 0 when DIP switch turned on. Controlled by APQ-GPIO 106	Default out of the box configuration is OFF
DMIC_DISC_N	S10-7	Disable (switch OFF) or Enable (switch ON) on-board DMICS	Default out of the box configuration is OFF
FORCE_SW_UART	S10-8	Option to select between use of DEBUG UART @ USB connector J22 (switch OFF) or onboard DMICs (switch ON)	Default out of the box configuration is OFF

Warning! Before making any changes to the dip switch, make sure to note down the previous configuration.

More details on boot configurations can be found in the Open-Q™ 624A SOM Device Specification document (R-3).

3.8.3 Power Input

The Open-Q™ development kit power source connects to the 12V DC power supply jack J21. Current Rating for this port is 3A. Starting from the power jack, the 12V power supply branches off into different voltage rails via step down converters on the carrier board and PMIC on the SOM. The SOM is powered by 3.9V via TI step down converter U400 on the carrier board or a single cell Li-on battery. To ensure the SOM is getting powered correctly, a user can monitor the current going into the SOM via the power probe header J86 (see section 3.8.7 below).

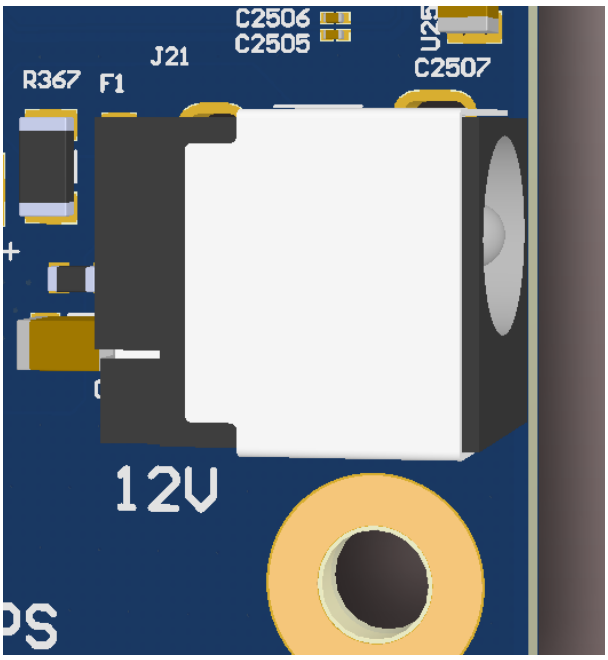

Figure 5 J21 12V DC Power Jack

The SOM includes 2 PMIC modules. Functionalities of the 2 modules are outlined below.

PMI8952 PMIC is used for:

- Sourcing various regulated power rails
- LCD Backlight / Bias Voltage Sourcing
- Battery charging

PM8953 PMIC is used for:

- Source various regulated power rails
- Source system clock

3.8.4 SOM Power Source Switch S300

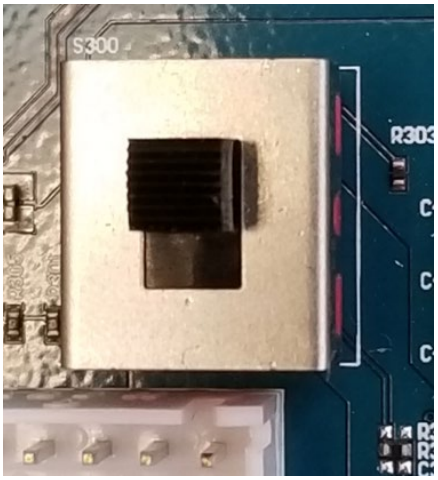

Figure 6 SOM Power Source Switch S300

The S300 switch allows the SOM to be powered from either a battery, or an onboard DC switching power supply (U400).

In the ‘UP’ position (as shown in the image above) the DC Power supply is the SOM Power source. In this state, BAT_THERM and BATT_ID must be simulated. Set Positions 3 and 4 of DIP Switch S1 to ‘ON’ (see below).

When the switch is in the ‘DOWN’ position, the DC source is from the battery connected to J300

3.8.5 Battery Dip Switch S1

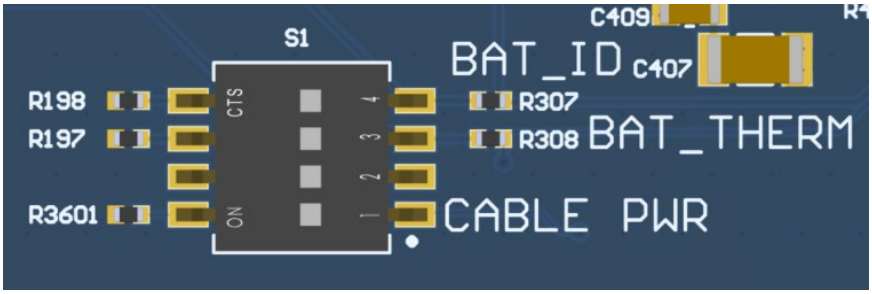

Figure 7 Battery Dip Switch S1

This 4-bit switch allows the user to control the battery configuration and boot options. Table 3-3 below outlines the pin outs and connections of this DIP switch.

Table 3-4 Battery DIP Switch S1 configuration

Function	Switch Position	Description	Notes
CBL_PWR_N	1	When switch is ON, platform will automatically boot when power is applied	Default out of the box configuration is ON
NC	2	No Function	
BAT_THERM	3	Turn switch ON to simulate battery thermistor, either when using a battery pack without thermistor, or when using onboard DC power supply instead of battery.	Default out of the box configuration is ON. See section 3.8.4 above for more details on switching between battery and onboard DC Power Supply.
BAT_ID	4	Turn switch ON to simulate battery ID, either when using a battery pack without a battery ID pin, or when using onboard DC power supply instead of battery.	Default out of the box configuration is ON. See section 3.8.4 above for more details on switching between battery and onboard DC Power Supply.

Warning! Before making any changes to the dip switch, make sure to note down the previous configuration.

3.8.6 Battery Connector J300

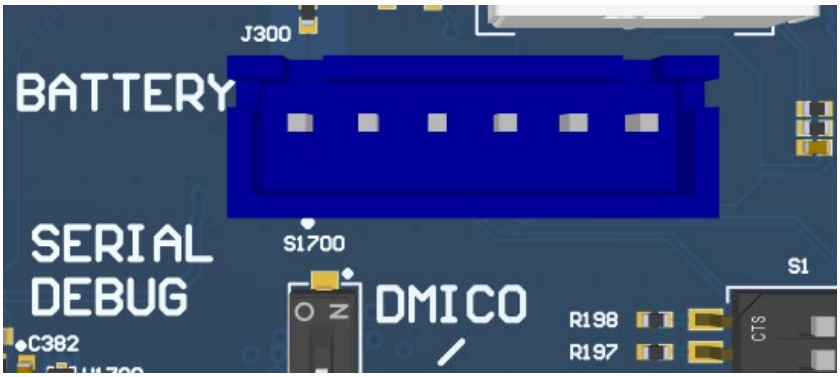

Figure 8 J300 Battery Connector

Table 3-5 Battery Connector Pinout J300

Function	Pin #	Description	Notes
VBATT_CONN	J300[6, 5]	Battery Voltage	Voltage must be 3.7V ~ 4.2V
BATT_ID_CONN	J300[4]	Battery Identification	Used for identification of battery pack type. Typically connects to a pull-down resistor in battery pack.
BAT_THERM_CONN	J300[3]	Battery Thermistor	Used for the charger to monitor the battery pack temperature.
GND	J300[1, 2]	Ground	

3.8.7 Power Probe Header J86

Figure 9 J86 Power Probe Header

The power probe header is used to sense/monitor the current on the 3.9V power rail going into the SOM (SOM_SYS_PWR). The table below summarizes the pin outs of header J86. A 0.005 Ohm sense resistor is connected between Pins 1 and 2. Refer to schematic for more details.

Table 3-6 Power Header J86 Pin-out

Description	Signal	Pin #
SOM power positive current sense line	SOM_PWR_SENSE_P	J86[1]
SOM power negative current sense line	SOM_PWR_SENSE_N	J86[2]
GND	GND	J86[3]

The SOM power consumption can be calculated with the formula below (where Rsense = 5 milliohms):

$$Psom = Vsom_{pwr_{sense_N}} * \frac{(Vsom_{pwr_{sense_P}} - Vsom_{pwr_{sense_N}})}{Rsense}$$

3.8.8 Power Header via 20 Pin Connector J60

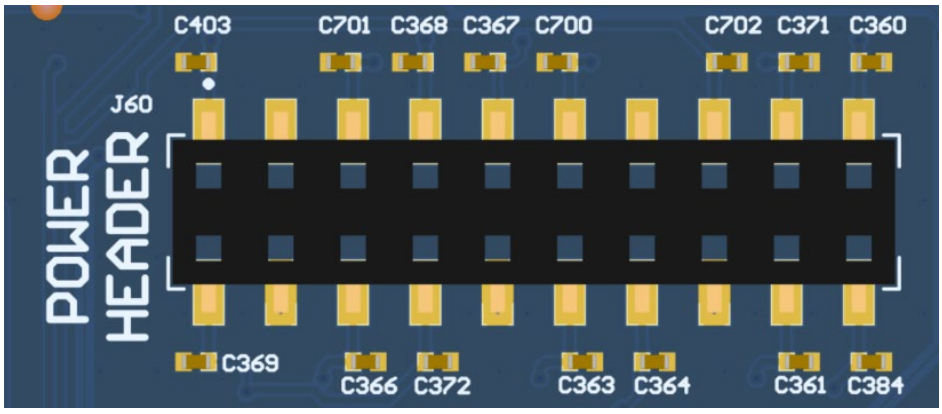

Figure 10 J60 Power Connector

- For providing camera connectors with additional current than what is originally supported by on board regulators.

- Can be used as a general power header if user would like to use voltage rails brought out by connector

Table 3-7. Power Header J60 Pin-out

Signal	Description	Pin #	Signal	Description	Pin #
MB_ELDO_CAM0_DVDD	1.1V power rail for camera 0. Max current draw 1A	J60[1]	VREG_L17_2P85	2.85V. Max current 300mA (Shared with Pin 2 and Both Camera connectors)	J60[2]
NC	NC	J60[3]	GND	GND	J60[4]
GND	GND	J60[5]	MB_VREG_3P3	3.3V	J60[6]
MB_ELDO_CAM1_DVDD	1.1V power rail for camera 1. Max current draw 1A	J60[7]	VREG_L17_2P85	2.85V. Max current 300mA (Shared with Pin 2 and Both Camera connectors)	J60[8]
MB_ELDO_CAM1_VCM	2.8V power rail for camera 1 (VDD). Max 300mA	J60[9]	GND	GND	J60[10]
GND	GND	J60[11]	MB_VREG_3P3	3.3V	J60[12]
NC	NC	J53[13]	VREG_L22_2P85	2.85V. Max Current 150mA	J60[14]
VREG_L11_SDC	2.95V Default. Max 800mA	J53[15]	GND	GND	J60[16]
VREG_L4_1P8	1.8V power rail for cameras 0 & 1. Max 300mA.	J60[17]	MB_VREG_3P3	3.3V	J60[18]
MB_VREG_5P0	5V power rail for cameras 0 & 1. Max 700mA	J60[19]	DC_IN_12V	12V	J60[20]

3.8.9 External Battery Charging Header J26

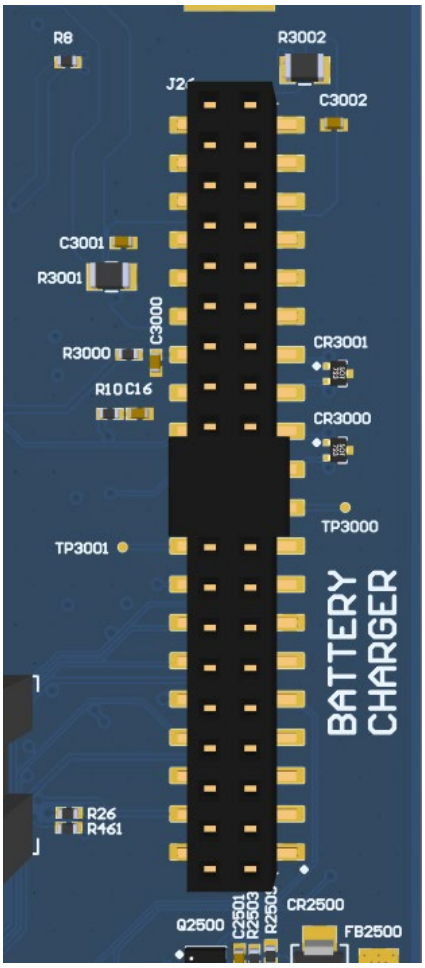

Figure 11 External Battery Charging Header J26

External battery charging header J26 breaks out signals to allow for charging of various types of external batteries.

Table 3-8. Power Header J26 Pin-out

Signal	Description	Pin #	Signal	Description	Pin #
GND	GND	J26[1]	GND	GND	J26[2]
BATT_P	Battery plus (+) terminal sense	J26[3]	PMI_VDD_CAP	LDO to supply fuel gauge circuits. Connect to bypass capacitor only, Do Not Load.	J26[4]
BATT_N	Battery minus (-) terminal sense	J26[5]	CHG_VBAT_SNS	Sensed battery voltage for charger circuits	J26[6]
BAT_ID	Battery ID, MIPI Battery interface, detects missing battery	J26[7]	PMI_CHG_EN	Charger Enable	J26[8]
BAT_THERM	Battery temperature input used by FG and by charger to ensure safe operation	J26[9]	SMB_PARALLEL_CHG_EN	SMB1350/SMB1351 enable for parallel charging	J26[10]
PM_VREG_BATT_THERM	Not Connected on Open-Q 624A SOM	J26[11]	SMB_INT	Leave Floating	J26[12]
GND	GND	J26[13]	SMB_STAT_N	Not Connected on Open-Q 624A SOM	J26[14]
PMI_GPIO_1	Software Configurable GPIO, WiPower long beacon extension (LBE) control	J26[15]	FG_ALARM	Not Connected on Open-Q 624A SOM	J26[16]
NC	NC	J26[17]	BATT_CHG_EXP_TP2	Testpoint 2	J26[18]
BATT_CHG_EXP_TP1	Testpoint 1	J26[19]	GND	GND	J26[20]
GPIO_5_BLSPx_UART_RX	UART RX	J26[21]	OPT_1	Leave Floating	J26[22]
GPIO_4_BLSPx_UART_TX	UART TX	J26[23]	OPT_2	Leave Floating	J26[24]
GPIO_7_BLSPx_I2C_SCL	I2C Clock	J26[25]	BATT_EXP_1P8	1.8V voltage supply	J26[26]
GPIO_6_BLSPx_I2C_SDA	I2C Data	J26[27]	GND	GND	J26[28]
GND	GND	J26[29]	BATT_EXP_SYS_PWR	Battery Voltage Supply	J26[30]
GND	GND	J26[31]	BATT_EXP_SYS_PWR	Battery Voltage Supply	J26[32]
GND	GND	J26[33]	BATT_EXP_SYS_PWR	Battery Voltage Supply	J26[34]
BATT_EXP_USB_VBUS	USB VBUS	J26[35]	GND	GND	J26[36]
BATT_EXP_USB_VBUS	USB VBUS	J26[37]	GND	GND	J26[38]
BATT_EXP_USB_VBUS	USB VBUS	J26[39]	GND	GND	J26[40]

3.8.10 Debug Serial UART over USB J22

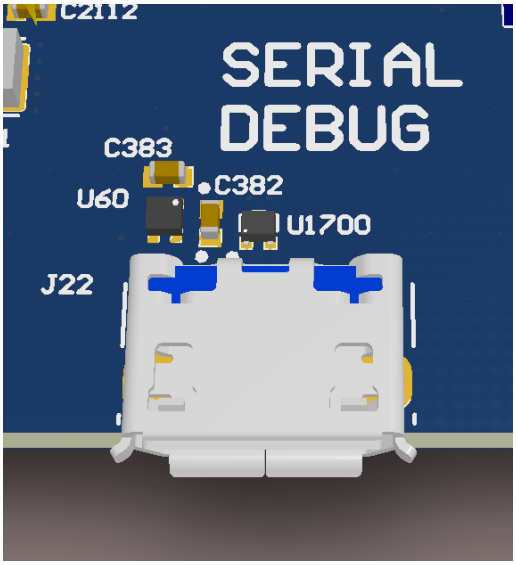

Figure 12 J22 Debug UART over USB

The UART connection used on the Open-Q 624A is a USB micro B connector (J22). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed.

Also, ensure the following DIP Switch is set:

DIP Switch S10 – Position 8 ‘FORCE_SW_UART’ Set to OFF/OPEN

The following table shows the serial configuration:

Table 3-9 Serial Debug Port Settings

Baud Rate	115200
Data Bits	8
Parity	none
Stop Bits	1
Flow Control	none

3.8.11 Sensor IO Expansion Header J53

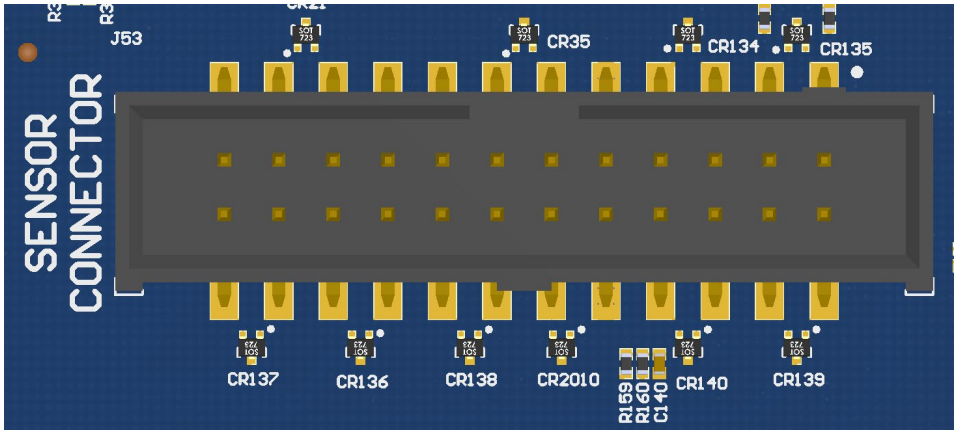

Figure 13 J53 Sensor Expansion Header

The sensor expansion header J53 allows for a 24-pin connection to an optional sensor board (ST Micro STEVAL-MKI128V6 sensor board). If user application does not require a sensor, then this header can be used for other applications that require UART/ SPI/ I2C/ UIM or GPIO input and output connections. Please refer to the schematic and consider power draw before connecting anything to this header.

Following is the pin breakout for sensor expansion header J53:

Table 3-10 Sensor Expansion Header J53 Pin out

Description	Signal	Pin #	Description	Signal	Pin #
Sensor I2C Bus – SDA (GPIO 6)	GPIO_6_BLSPx_I2C_SDA	J53[1]	Accelerometer interrupt input to processor via GPIO42	SENSOR_ACCEL_INT	J53[2]
Sensor I2C Bus – SCL (GPIO 7)	GPIO_7_BLSPx_I2C_SCL	J53[3]	Cap interrupt input to processor via GPIO65	SENSOR_CAP_INT_N	J53[4]
Sensor reset signal from processor to sensor via GPIO127	GPIO_XX_SENSOR_RST	J53[5]	Gyroscope interrupt input to processor via GPIO45 *NOTE: Not populated by default.	SENSOR_GYRO_INT	J53[6]
Sensor IO PWR 1.8 V VREG_L6_1P8 power supply regulator (Digital)	VREG_L6_1P8	J53[7]	Sensor Analog power supply from VREG_L10_3P0. 3.0V or 3.3V (If R160 populated, R159 removed)	SENS_ANA_PWR	J53[8]
GND	GND	J53[9]	GND	GND	J53[10]
HRM interrupt/ configurable GPIO140	SENSOR_HRM_INT	J53[11]	Touch screen interrupt input from processor via GPIO13	TS_INT_N	J53[12]
Magnetic Switch Interrupt input to processor via GPIO48	GPIO_48_SPI6_CS1_MAG_N	J53[13]	Alternate sensor interrupt input to processor via GPIO43	SENSOR_ALSP_INT_N	J53[14]
NC	NC	J53[15]	Digital Compass interrupt input to processor via GPIO44. *NOTE: Not populated by default.	SENSOR_MAG_DRDY_INT	J53[16]
NC	NC	J53[17]	Pressure Sensor interrupt input to processor via GPIO46. *Note, by default, this pin is used for another purpose. To use for this purpose, remove R311.	GPIO_XX_PRESSURE_INT	J53[18]

Description	Signal	Pin #	Description	Signal	Pin #
Sensor SPI Bus – Chip Select (GPIO48)	SSC_SPI_1_CS_N	J53[19]	Sensor SPI Bus – MOSI (GPIO20)	BLSP6_3_SPI_MOSI	J53[20]
Sensor SPI Bus – CLK (GPIO23)	SSC_SPI_1_CLK	J53[21]	Sensor SPI Bus – MISO (GPIO21)	BLSP6_2_SPI_MISO	J53[22]
NC	NC	J53[23]	GPIO 35	CCI_TIMER2	J53[24]

3.8.12 Audio Input Expansion Header J50

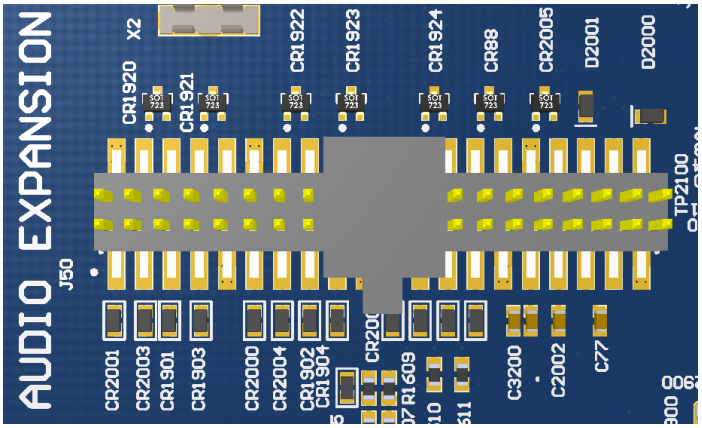

Figure 14 Audio Input Expansion Header J50

This 40-pin expansion header provides the following audio inputs/outputs:

- 4 digital mic channels (supports 8 mics)
- 4 analog mics
- Voltage rails to support analog and digital mics
- 2 single ended analog audio line out
- 3 GPIO's

*Note, availability of DMICs on this header depends on configuration of DIP Switch S10. See section 3.8.2 for more details. To use DMICs on this header, on-board DMICs must first be disabled by setting S10 position 7 (DMIC_DISC_N) to OFF/OPEN.

The table below outlines the pin out information of the audio outputs expansion header J50:

Table 3-11 Audio Expansion Header J50 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog MIC1 positive differential input	CDC_MIC1_P	J50[1]	GND	GND	J50[2]
Analog MIC1 negative differential input	CDC_MIC1_N	J50[3]	Connects to SOM DMIC CLK Input (GPIO 89)	624_DMIC0_CLK	J50[4]
Analog MIC2 positive differential input	CDC_MIC2_P	J50[5]	Connects to SOM DMIC DATA Input (GPIO 90)	624_DMIC0_DATA	J50[6]
Analog MIC2 negative differential input	CDC_MIC2_N	J50[7]	CLK for Dual DMICs on Channel 1 (U1601 & U1602)	CDC_DMIC1_CLK	J50[8]
GND	GND	J50[9]	DATA for Dual DMICs on Channel 1 (U1601 & U1602)	CDC_DMIC1_DATA	J50[10]
Analog MIC3 positive differential input	CDC_MIC3_P	J50[11]	GND	GND	J50[12]
Analog MIC3 negative differential input	CDC_MIC3_N	J50[13]	CLK for Dual DMICs on Channel 2 (U1603 & U1604)	CDC_DMIC2_CLK	J50[14]
Analog MIC4 positive differential input	CDC_MIC4_P	J50[15]	DATA for Dual DMICs on Channel 2 (U1603 & U1604)	CDC_DMIC2_DATA	J50[16]
Analog MIC4 negative differential input	CDC_MIC4_N	J50[17]	CLK for Dual DMICs on Channel 3 (U1605 & U1606)	CDC_DMIC3_CLK	J50[18]
GND	GND	J50[19]	DATA for Dual DMICs on Channel 3 (U1605 & U1606)	CDC_DMIC3_DATA	J50[20]
Mic Bias output voltage 1	CDC_MIC_BIAS1	J50[21]	GND	GND	J50[22]
Mic Bias output voltage 2	CDC_MIC_BIAS2	J50[23]	PMI 8951 GPIO 1. Configurable.	PMI_GPIO_1	J50[24]
Mic Bias output voltage 3	CDC_MIC_BIAS3	J50[25]	CLK for Dual DMICs on Channel 0 (U1609 & U1610).	212_DMIC0_CLK	J50[26]
Mic Bias output voltage 4	CDC_MIC_BIAS4	J50[27]	DATA for Dual DMICs on Channel 0 (U1609 & U1610).	212_DMIC0_DATA	J50[28]
GND	GND	J50[29]	Input.	GPIO_MIC_MUTE_ STATUS	J50[30]
1.8V output power supply	VREG_L5_1P8	J50[31	GND	GND	J50[32]

Description	Signal	Pin NO	Description	Signal	Pin NO
		]			
3.3V output power supply	MB_VREG_3P3	J50[33]	GPIO 117	GPIO_XX_MIC_SEL ECT	J50[34]
5.0V output power supply	MB_VREG_5P0	J50[35]	Analog audio line out 3, single ended output	CDC_LINE_OUT_3	J50[36]
NC	No Net	J50[37]	Audio line outputs 3 and 4 GND reference	CDC_LINE_OUT_R EF	J50[38]
GND	GND	J50[39]	Analog audio line out 4, single ended output	CDC_LINE_OUT_4	J50[40]

3.8.13 3.5mm Headphone and Microphone Jack J27

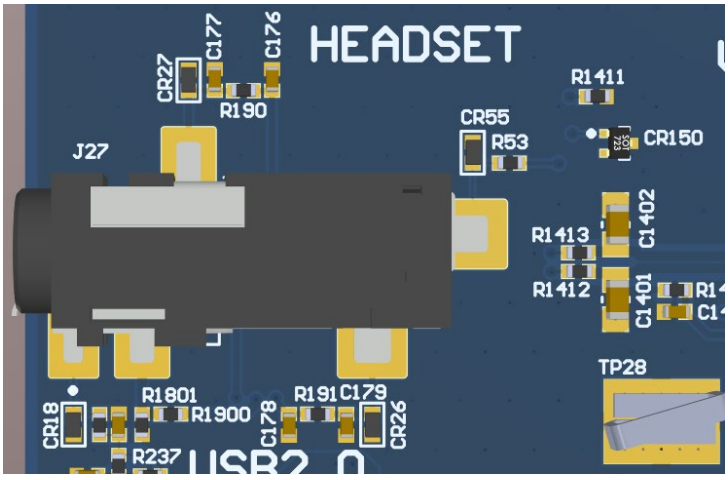

Figure 15 3.5mm Headphone and Microphone Jack J27

The on-board 3.5mm TRRS jack provides capabilities for a headset with microphone. The headphone jack follows standard CTIA / AHJ standard pinout.

3.8.14 Stereo Speaker Header J2100

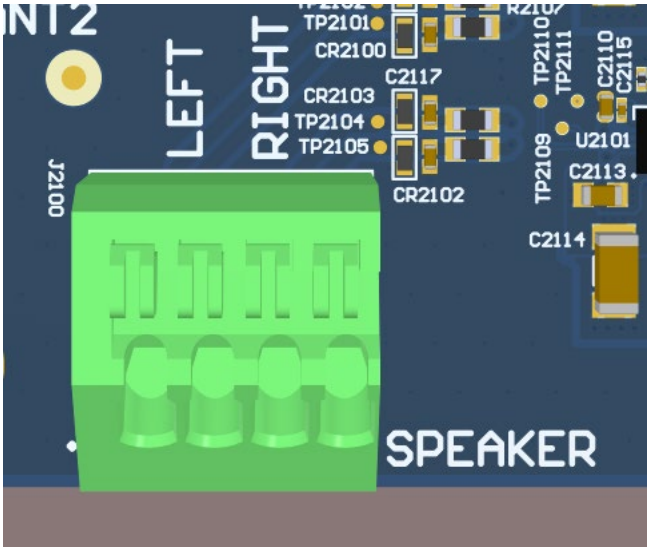

Figure 16 Stereo Speaker Header J2100

Output from two WSA8815 amplifiers are available at J2100. The WSA8815 amplifiers can deliver up to 4.0 W into an 8 Ω load with 1% THD. Speaker impedances of 4 Ω to 8 Ω are supported.

Table 3-12 Stereo Speaker Header J2100

Description	Signal	Pin NO
Speaker Left Channel (-)	WSA_SPKR_L_N	J2100[1]
Speaker Left Channel (+)	WSA_SPKR_L_P	J2100[2]
Speaker Right Channel (-)	WSA_SPKR_R_N	J2100[3]
Speaker Right Channel (+)	WSA_SPKR_R_P	J2100[4]

3.8.15 External Codec/GPIO Expansion Header J1

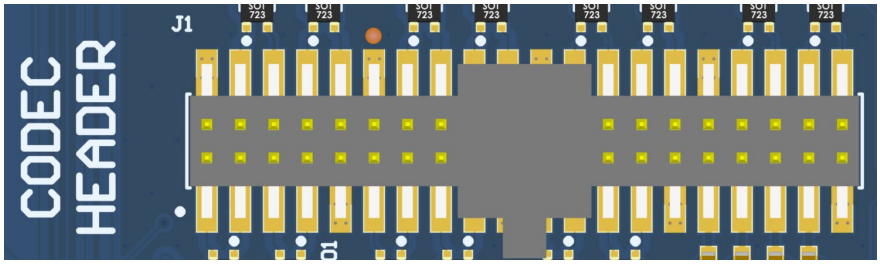

Figure 17 External Codec/GPIO Expansion Header J1

This header exposes GPIO and other signals not exposed or used elsewhere in the platform. It also supports the use of an external audio codec/amplifier through I2S interfaces, as well as supplying power.

Table 3-13 External Codec/GPIO Expansion Header J1 Pin out

Description	Signal	Pin #	Description	Signal	Pin #
BLSP1 bit 3 - SPI1_MOSI (GPIO 0)	GPIO_0_BLSP1_SPI_MOSI	J1[1]	GND	GND	J1[2]
BLSP1 bit 2 - SPI1_MISO (GPIO 1)	GPIO_1_BLSP1_SPI_MISO	J1[3]	PMIC GPIO 1 – Intended use is for 9.6Mhz CODEC MCLK (DIV_CLK2)	PM_GPIO_1_DIV_CLK2	J1[4]
BLSP1 bit 1 - SPI1_CS or I2C1_SDA (GPIO 2)	GPIO_2_BLSP1_SPI_CS_N	J1[5]	PMIC Multi-Purpose Pin 3	PM_MPP_3	J1[6]
BLSP1 bit 0 - SPI1_CLK or I2C1_SCL (GPIO 3)	GPIO_3_BLSP1_SPI_CLK	J1[7]	MI2S Bus 1 – Data bit 3 (GPIO 95)	MI2S_1_D3	J1[8]
GND	GND	J1[9]	MI2S Bus 1 – Data bit 2 (GPIO 94)	MI2S_1_D2	J1[10]
GPIO 74 – Intended use is for codec interrupt input	WCD_INT	J1[11]	GND	GND	J1[12]
Slimbus Data Bit 1 – For Codec connection (GPIO 72)	B2B_SLIMBUS_DATA1	J1[13]	MI2S Bus 1 – Data bit 1 (GPIO 88)	MI2S_1_D1	J1[14]
Slimbus Data Bit 0 – For Codec connection (GPIO 71)	B2B_SLIMBUS_DATA0	J1[15]	MI2S Bus 1 – Data bit 0 (GPIO 93)	MI2S_1_D0	J1[16]
Slimbus CLK– For Codec connection (GPIO 70)	B2B_SLIMBUS_CLK	J1[17]	MI2S Bus 1 – WS (GPIO 92)	MI2S_1_WS	J1[18]
GND	GND	J1[19]	MI2S Bus 1 – SCK (GPIO 91)	MI2S_1_SCK	J1[20]

Description	Signal	Pin #	Description	Signal	Pin #
MI2S Bus 2 – Data bit 1 (GPIO 138) **Note** shared with HDMI Connector. Connected to this connector by default. Connect to HDMI by turning DIP SW S2 to 'ON'	MI2S_2_D1_HDR	J1[21]	GND	GND	J1[22]
MI2S Bus 2 – Data bit 0 (GPIO 137) **Note** shared with HDMI Connector. Connected to this connector by default. Connect to HDMI by turning DIP SW S2 to 'ON'	MI2S_2_D0_HDR	J1[23]	General Purpose. GPIO 96	GPIO_96_OR_53	J1[24]
MI2S Bus 2 – WS (GPIO 136) **Note** shared with HDMI Connector. Connected to this connector by default. Connect to HDMI by turning DIP SW S2 to 'ON'	MI2S_2_WS_HDR	J1[25]	General Purpose. GPIO 98	GPIO_98_OR_55	J1[26]
MI2S Bus 2 – SCK (GPIO 135) **Note** shared with HDMI Connector. Connected to this connector by default. Connect to HDMI by turning DIP SW S2 to 'ON'	MI2S_2_SCK_HDR	J1[27]	Enables on-board amplifiers. May be used to enable external amplifiers/devices. (GPIO 68)	GPIO_68_AMP_PWR_EN	J1[28]
GND	GND	J1[29]	Primary MI2S master clock A (GPIO 25)	GPIO_25_MI2S_MCLK	J1[30]
+1.8V Power. 150mA Current Limit	VREG_L5_1P8	J1[31]	GND	GND	J1[32]
+3.3V Power. Shared with system.	MB_VREG_3P3	J1[33]	Not Connected	212_GPIO_75	J1[34]
+5.0V Power. Shared with system.	MB_VREG_5P0	J1[35]	Not Connected	212_GPIO_84	J1[36]
+12V Power. Shared with system.	DC_IN_12V	J1[37]	GPIO 45	GPIO_45_AMP_FAULT	J1[38]
GND	GND	J1[39]	GPIO 44	GPIO_44_AMP_RST_N	J1[40]

3.8.16 On Board Digital Mics

The Open-Q™ 624A carrier board has 8 on board Digital Microphones, located on the bottom of the board. The microphones are Knowles SPK0415HM4H-B-7 [100Hz ~ 10kHz Digital, PDM Microphone MEMS (Silicon) Omnidirectional (-26dB ±3dB @ 94dB SPL)]

*Note, availability of onboard DMICs depends on configuration of DIP Switch S10. See section 3.8.2 for more details. To use onboard DMICs set S10 position 7 (DMIC_DISC_N) to ON.

DMIC Channel	Microphones
CDC_DMIC1 (WCD9335)	U1601, U1602
CDC_DMIC2 (WCD9335)	U1603, U1604
CDC_DMIC3 (WCD9335)	U1605, U1606
624_DMIC0 (APQ Processor DMIC, GPIO 89/90)	U1609, U1610

3.8.17 On Board PCB Wi-Fi and BT Antennas

The Open-Q™ 624A carrier board has two on-board Wi-Fi PCB antennas and one on-board Bluetooth antenna that connects to the Wi-Fi/BT module on the SOM via coaxial cables. These antennas connect to the SOM in the following configuration:

- WLAN ANT1 on the carrier board connects through coax connector J9 to MH4F connector ANT0 on the Wi-Fi/BT module
- WLAN ANT2 on the carrier board connects through coax connector J8 to MH4F connector ANT1 on the Wi-Fi/BT module
- BT ANT on the carrier board connects through coax connector J7 to MH4F connector BT on the Wi-Fi/BT module

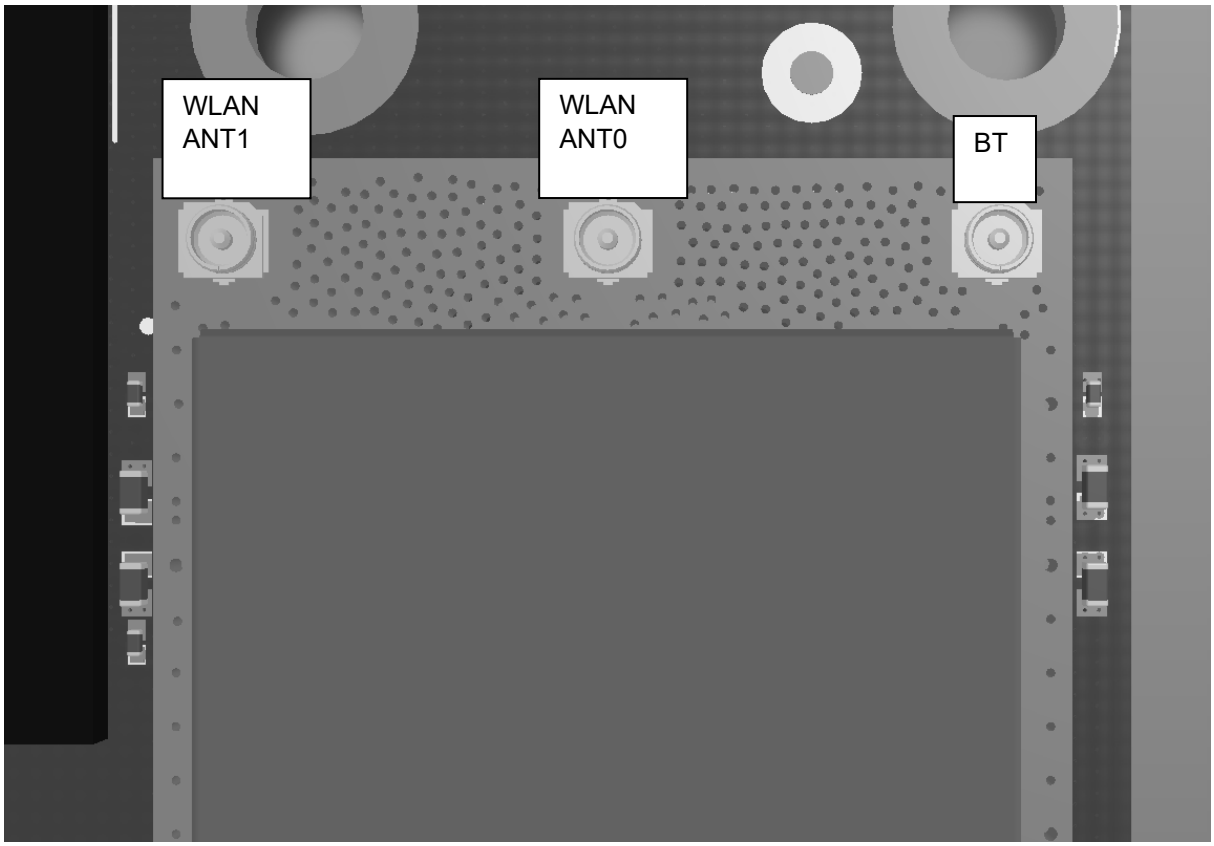

Figure 18 Wi-Fi/BT Module Antenna Connectors

3.8.18 GNSS Front-end and Antennas

The Open-Q™ 624A carrier board includes a GNSS RF front-end circuit as well as a PCB trace antenna and an SMA type external antenna connector. The RF front-end circuit includes an LNA and a SAW filter for improved performance and an antenna switch to enable connection to either the PCB trace antenna or the SMA external antenna connector. Depending on which antenna is used, DIP switch S10 must be configured correctly (see Table 3-14 below for details).

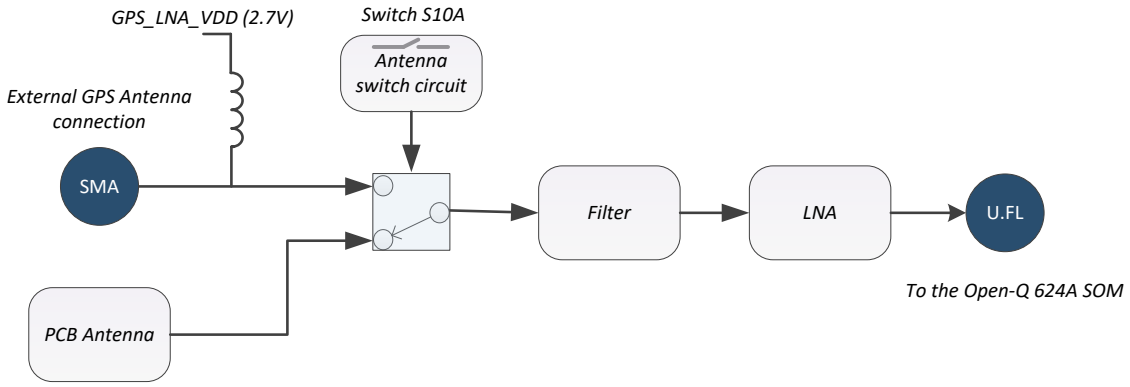

Figure 19 GNSS Front-end block diagram.

Table 3-14 GNSS Antenna Selection Switch

GPS Antenna Selection [GPS_CTRL1]	DIP Switch S10 (Position 1) Selection
On Board PCB Antenna	OFF
External Antenna	ON

PCB Trace Antenna: Note that the PCB trace antenna has relatively low performance and will generally only provide sufficient signal quality if there is a clear open view of the sky. Otherwise, a better, external antenna connected to the SMA connector will be required.

Use of External Antenna: A passive or active antenna may be connected to the SMA external antenna connector, but it is recommended to use an active antenna unless the antenna cable is very short, or the antenna is connected directly to the SMA connector. If the antenna cable is long, the signal loss through the cable will seriously degrade the signal level unless an active antenna is used. The antenna port is biased with 2.7v specifically for powering an active antenna so make sure to select an antenna that can operate from 2.7v.

Evaluation of GNSS Receiver Performance: Note that the performance of the GNSS receiver will be affected significantly by the following factors:

- Whether or not an active antenna is used
- The gain and directionality of the antenna
- Whether the RF front-end of the carrier board is used.

Therefore, if the goal is to evaluate the GNSS receiver performance of the SOM with a user-selected antenna intended for an end product, it should be connected directly to the SOM's GPS antenna connector (U.FL) to eliminate the effects of the LNA, filter, and coax cable losses on the carrier board.

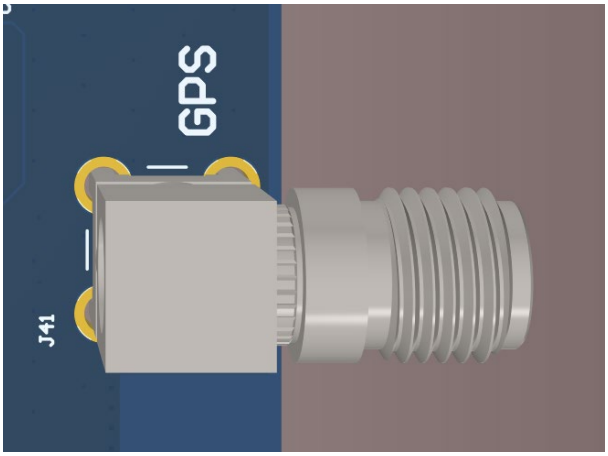

Figure 20 GNSS External Antenna Connector

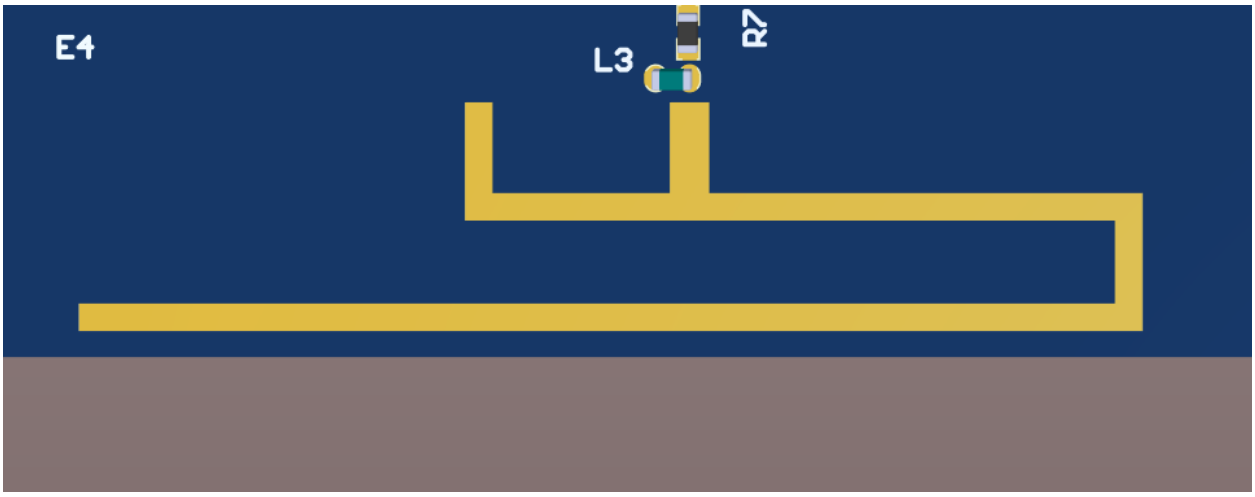

Figure 21 Onboard GNSS Antenna

3.8.19 Display Connector J2

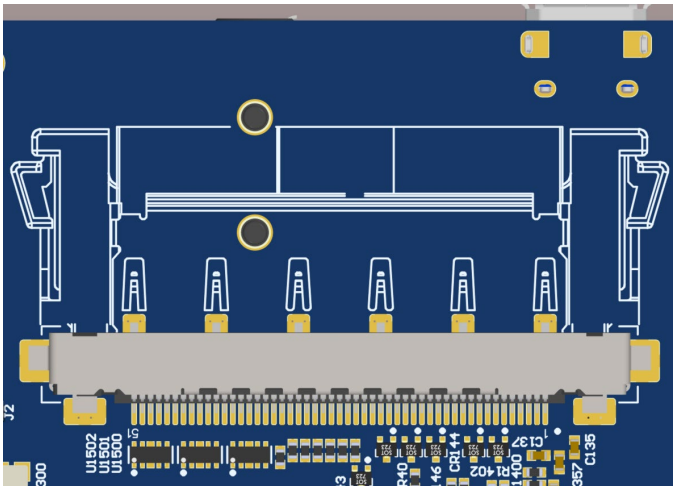

Figure 22 Display Connector J2

The 51-pin display connector provides the following features/ pin-outs that enables the development kit to connect to a MIPI DSI panel/ device:

Note: Please refer to the carrier board schematic and display board tech notes when designing a custom display board.

- DSI
  - 4 lane MIPI DSI - FHD (1920 × 1200) 60 fps
- Backlight
  - Built-in backlight WLED driver on PMI8952
    - WLED driver supports four LED strings of up to 20mA each with 28V maximum boost voltage (with 2 strings, or 24V with 4 strings)
  - External Backlight Driver Support
    - Backlight control signals
    - External Power
- Display connector – LCD/ AMOLED
  - PMI8952 programmable display bias output voltage:
    - 5V to 6.1V and -1.4V to -6.0V (LCD display)
    - 4.6V to 5V and -1.4V to -5.4V (AMOLED display)
- Additional GPIOs for general purposes available
- Touch Panel
  - Supports up to two touch screen controllers
  - Supports I2C or SPI via BLSP3

Note: An optional 4.5” LCD/touchscreen accessory is available for the Open-Q 624A development kit. See section 0 below for more information. To purchase this, please visit http://shop.intrinsyc.com or contact Lantronix at sales@lantronix.com for details.

Pin #	Signal	Description
J2[1]	GND	GND
J2[2]	VREG_L5_1P8	Power output. Connected to PM8953 VREG_L5 regulator. Default is +1.8V. Maximum current 600mA (shared with other platform circuitry)
J2[3]	VREG_L10_3P0	Power output. Connected to PM8953 VREG_L5 regulator. Default is +3.0V. Maximum current 150mA
J2[4]	V_LCD_BACKLIGHT_CONN	+12V DC Power Output
J2[5]	V_LCD_BACKLIGHT_CONN	
J2[6]	PM_MPP_4_WLED_PWM_CTRL	PWM output dimming control on external backlight driver (PM8953 MPP 4)
J2[7]	NC	No Connection
J2[8]	BLSPy_1_TS_I2C_SDA	BLSP3 Bit 1 - SPI3_CS / I2C3_SDA (APQ_GPIO_10)
J2[9]	NC	No Connection
J2[10]	BLSPy_2_UART_RX	BLSP3 Bit 2 - SPI3_MISO (APQ_GPIO_9)
J2[11]	BLSPy_0_TS_I2C_SCL	BLSP3 Bit 0 - SPI3_CLK / I2C3_SCL (APQ_GPIO_11)
J2[12]	VREG_L6_1P8	Power output. Connected to PM8953 VREG_L6 regulator. Default is +1.8V. Maximum current 300mA (shared with other platform circuitry)
J2[13]	BLSPy_3_UART_TX	BLSP3 Bit 3 - SPI3_MOSI (APQ_GPIO_8)
J2[14]	TS_INT_N	Input, Touchscreen Interrupt (APQ_GPIO_65)
J2[15]	BACKLIGHT_EN_CONN	Output, Backlight Enable (APQ_GPIO_100)
J2[16]	DISP_MDP_VSYNC_P	Output, SDE vertical sync – primary (APQ_GPIO_24)
J2[17]	NC	No Connection
J2[18]	NC	No Connection
J2[19]	DISP_MDP_VSYNC_S	Output, SDE vertical sync – secondary (APQ_GPIO_25)
J2[20]	NC	No Connection
J2[21]	NC	No Connection
J2[22]	TS0_RESET_N	Output, Touchscreen Reset (APQ_GPIO_64)
J2[23]	NC	No Connection
J2[24]	WLED_CABC_DISP	PWM input for dynamic dimming (Content Adaptive Backlight Control)
J2[25]	GND	GND

Pin #	Signal	Description
J2[26]	VOUT_WLED_DISP	Backlight LED Voltage Output
J2[27]	WLED_SINK1_DISP	Backlight LED String 1 Current Sink. Max 30mA
J2[28]	GND	GND
J2[29]	WLED_SINK2_DISP	Backlight LED String 2 Current Sink. Max 30mA
J2[30]	WLED_SINK3_DISP	Backlight LED String 3 Current Sink. Max 30mA
J2[31]	GND	GND
J2[32]	WLED_SINK4_DISP	Backlight LED String 4 Current Sink. Max 30mA
J2[33]	MB_VREG_3P3_DISP	+3.0V Power output. Maximum current 150mA
J2[34]	GND	GND
J2[35]	VREG_DISP_5V_P_DISP	Display Bias, Positive. Default +5.5V
J2[36]	VREG_DISP_5V_N_DISP	Display Bias,Negative. Default -5.5V
J2[37]	GND	GND
J2[38]	MIPI_DSI0_DATA3_CONN_N	MIPI DSI Data Channel 3 Output Negative Lane
J2[39]	MIPI_DSI0_DATA3_CONN_P	MIPI DSI Data Channel 3 Output Positive Lane
J2[40]	GND	GND
J2[41]	MIPI_DSI0_DATA2_CONN_N	MIPI DSI Data Channel 2 Output Negative Lane
J2[42]	MIPI_DSI0_DATA2_CONN_P	MIPI DSI Data Channel 2 Output Positive Lane
J2[43]	GND	GND
J2[44]	MIPI_DSI0_DATA1_CONN_N	MIPI DSI Data Channel 1 Output Negative Lane
J2[45]	MIPI_DSI0_DATA1_CONN_P	MIPI DSI Data Channel 1 Output Positive Lane
J2[46]	LCD_RESET_N	Output, LCD Reset (APQ_GPIO_61)
J2[47]	MIPI_DSI0_DATA0_CONN_P	MIPI DSI Data Channel 0 Output Positive Lane
J2[48]	MIPI_DSI0_DATA0_CONN_N	MIPI DSI Data Channel 0 Output Negative Lane
J2[49]	DISPLAY_GP2_GND	Connected to GND by default
J2[50]	MIPI_DSI0_CLK_CONN_P	MIPI DSI Clock Output Positive Lane
J2[51]	MIPI_DSI0_CLK_CONN_N	MIPI DSI Clock Output Negative Lane

3.8.20 Camera connectors J4 and J5

The Open-Q 624A development kit supports two 4-lane MIPI camera interfaces via three separate JAE 41-pin connectors.

The following are some features of the camera connectors:

- 2 x 4 lane MIPI CSI signals
- No support for integrated flash driver
- CSI connectors are on the carrier board edge
- Self-regulated camera modules can be powered with 3.3V power (MB_VREG_3P3)
- Uses JAE FI-RE41S-HF connector for exposing MIPI, CLK, GPIOs and Power rails.

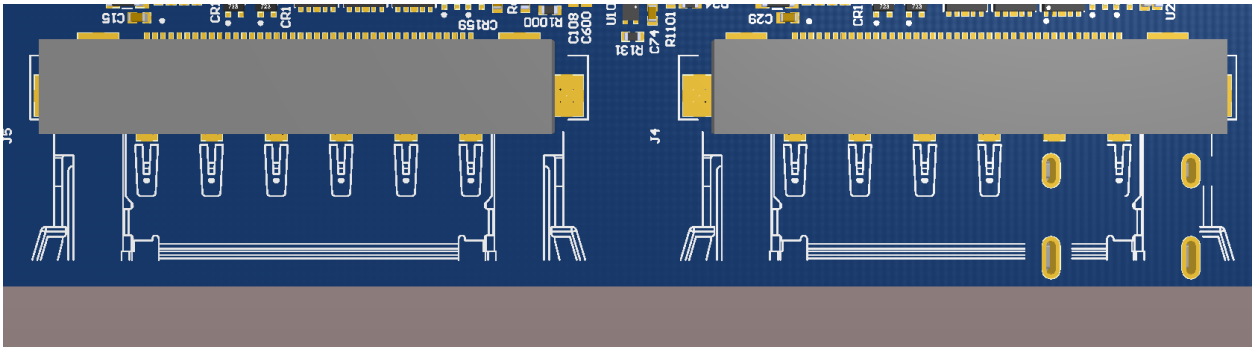

Figure 23 Camera Connectors (J4, J5)

Figure 21 above shows the MIPI CAM0 (J5) and CAM1 (J4) and connectors. Table 3-15 below outlines the pin outs of these connectors

Table 3-15. MIPI CSI Camera Connector Pinouts (J5, J4)

Pin #	CAM0(J5)	CAM1(J4)	Description
1	MB_VREG_3P3	MB_VREG_3P3	Power output. Connected to main +3.3V MB_VREG_3P3 max current 700mA
2	MB_VREG_3P3	MB_VREG_3P3	
3	MB_VREG_3P3	MB_VREG_3P3	
4	GND	GND	Ground
5	VREG_L17_2P85	VREG_L17_2P85	Power output. Connected to PM8953 VREG_L17 regulator. Default is +2.85V. Maximum current 300mA (shared between cameras)
6	MB_ELDO_CAM0_DVDD	MB_ELDO_CAM1_DVDD	Power output. +1.1V Default. Maximum current 300mA. Option to source from onboard LDOs (1A max current) instead of SOM LDO VREG_L2

Pin #	CAM0(J5)	CAM1(J4)	Description
7	VREG_L22_2P8	MB_ELDO_CAM1_VCM	Power output. Connected to PM8953 VREG_L22 regulator (150mA) on CAM0, and onboard LDO (300mA) on CAM1. Default is +2.80.
8	VREG_L22_2P8	MB_ELDO_CAM1_VCM	
9	VREG_L6_1P8	VREG_L6_1P8	Power output. Connected to PM8953 VREG_L6_1P8. Default is +1.8V. Maximum current 300mA
10	VREG_L6_1P8	VREG_L6_1P8	
11	GPIO_CAM_MUTE_STATUS (APQ_GPIO87)	GPIO_CAM_MUTE_STATUS (APQ_GPIO87)	Default Use is for camera shutter closed indication. Connected to GND on Lantronix Camera Adaptor Boards.
12	CAM0_FLASH_EN (APQ_GPIO33)	CAM1_FLASH_EN (APQ_GPIO33)- Not connected by Default	Output. Default use is for camera flash strobe enable
13	CAM1_RST_N (APQ_GPIO40)	CAM2_RST_N (APQ_GPIO129)	Output. Default use is for camera reset
14	CAM1_STANDBY_N (APQ_GPIO39)	CAM2_STANDBY_N (APQ_GPIO130)	Output. Default use is for camera standby
15	GPIO_30_CCI_I2C_SCL0 (APQ_GPIO30)	GPIO_30_CCI_I2C_SCL0 (APQ_GPIO30)	Output. Default use is for camera CCI0 I2C clock interface
16	GPIO_29_CCI_I2C_SDA0 (APQ_GPIO29)	GPIO_29_CCI_I2C_SDA0 (APQ_GPIO29)	Input / output. Default use is for camera CCI0 I2C data interface
17	GPIO_26_CAM_MCLK0 (APQ_GPIO26)	GPIO_27_CAM_MCLK1 (APQ_GPIO27)	Output. Default use is for camera master clock. Maximum 24MHz
18	CAM0_FLASH_TRIG (APQ_GPIO34)	CAM0_FLASH_TRIG (APQ_GPIO34)- Not connected by Default	Output. Default use is for camera flash strobe trigger
19	GND	GND	Ground
20	MIPI_CSI0_LANE0_N	MIPI_CSI1_LANE0_N	Input. MIPI CSI0 / CSI1data lane 0
21	MIPI_CSI0_LANE0_P	MIPI_CSI1_LANE0_P	Input. MIPI CSI0 / CSI1 data lane 0
22	GND	GND	Ground

Pin #	CAM0(J5)	CAM1(J4)	Description
23	MIPI_CSI0_CLK_N	MIPI_CSI1_CLK_N	Input. MIPI CSI0 / CSI1 clock lane
24	MIPI_CSI0_CLK_P	MIPI_CSI1_CLK_P	Input. MIPI CSI0 / CSI1 clock lane
25	GND	GND	Ground
26	MIPI_CSI0_LANE1_N	MIPI_CSI1_LANE1_N	Input. MIPI CSI0 / CSI1 data lane 1
27	MIPI_CSI0_LANE1_P	MIPI_CSI1_LANE1_P	Input. MIPI CSI0 / CSI1 data lane 1
28	GND	GND	Ground
29	MIPI_CSI0_LANE2_N	MIPI_CSI1_LANE2_N	Input. MIPI CSI0 / CSI1 data lane 2
30	MIPI_CSI0_LANE2_P	MIPI_CSI1_LANE2_P	Input. MIPI CSI0 / CSI1 data lane 2
31	GND	GND	Ground
32	MIPI_CSI0_LANE3_P	MIPI_CSI1_LANE3_P	Input. MIPI CSI0 / CSI1 data lane 3
33	MIPI_CSI0_LANE3_N	MIPI_CSI1_LANE3_N	Input. MIPI CSI0 / CSI1 data lane 3
34	GND	GND	Ground
35	GPIO_31_CCI_I2C_SDA1 (APQ_GPIO31)	GPIO_31_CCI_I2C_SDA1 (APQ_GPIO31)	Output / Input. Default use is for camera CCI1 I2C data interface
36	GPIO_32_CCI_I2C_SCL1 (APQ_GPIO32)	GPIO_32_CCI_I2C_SCL1 (APQ_GPIO32)	Output. Default use is for camera CCI1 I2C clock interface
37	CAM_IRQ (APQ_GPIO12)	CAM_IRQ (APQ_GPIO12) - Not connected by Default	Input. CAM_IRQ signal
38	CAM0_MCLK3 (APQ_GPIO128)	CAM1_MCLKX_CONN (APQ_GPIO28)	Output. Default use is for camera master clock. Maximum 24MHz
39	MB_ELDO_CAM0_DVDD	MB_ELDO_CAM1_DVDD	Power output. +1.1V Default. Maximum current 300mA. Option to source from onboard LDOs (1A max current) instead of SOM LDO VREG_L2
40	MB_VREG_5P0	MB_VREG_5P0- Not connected by Default	Power output. 5V Power supply. Maximum 700mA

Pin #	CAM0(J5)	CAM1(J4)	Description
41	MB_VREG_5P0	MB_VREG_5P0- Not connected by Default	

Note: A connection from the camera connectors on the carrier board to the camera adapter board is established by a 41-pin cable assembly from JAE Electronics (part number JF08R0R041020MA)

An optional Camera Module Accessory is available. See Section 3.9.1 below for more details.

3.8.21 Automation Connector Header J3100

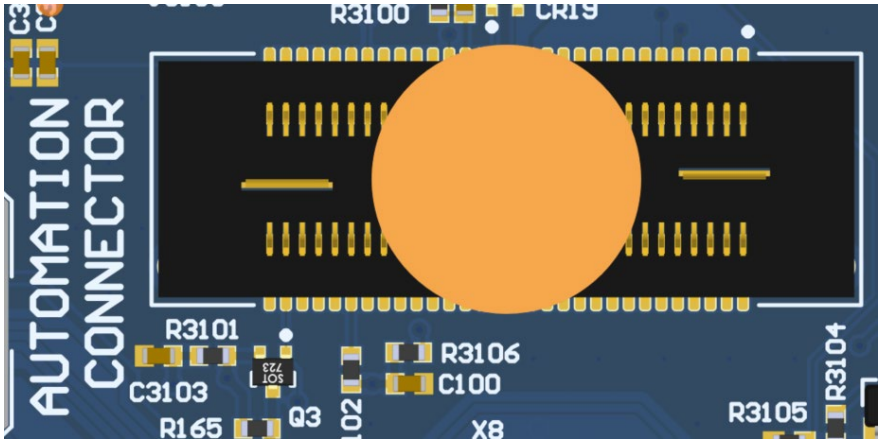

Figure 24 J3100 Automation connector header

This 60-pin header is used for automating tests on the development platform. Such tests include powering on and off and managing automated software downloads on the board. If automation is not required, user can access free GPIO pins from this header. Table 3-16 below outlines the pins that are available via header J3100. Please refer to carrier and SOM schematics for details on where signals are connected to. *Note, if this connector is to be used, remove R300 and disable battery source using switch S300 (see section 3.8.4 above for details on battery switch)

Table 3-16. Automation Connector J3100 Pin Out

***Note most pins on this connector are Not Connected. Only connected pins are listed.**

Description	Signal	Pin #	Description	Signal	Pin #
+1.8V power output from LDO VREG_L5_1P8	VREG_MDM_1P8	9	Connected to LDO VREG_L5_1P8	PLATFORM_ID	50
Power supply hold signal output from APQ to PMIC	APQ_PS_HOLD	11	Reset output from APQ	APQ_RESOUT_N	58
Input used to disconnect VBUS from USB Ports. Active High.	USB_VBUS_DISBL	27			
Power Button input	KYPD_PWR_N	29			
Reset Button input	RESIN_N	31			
+12V Rail	AUTO_12V	35			
Reset output from PMIC	PM_PON_RESET_N	37			
Input. High to enter USB BOOT mode	FORCED_USB_BOOT	47			

Description	Signal	Pin #	Description	Signal	Pin #
Input. +3.9V System Power for SOM.	AUTO_VBATT	49 51 53 55 57 59			

3.8.22 Buttons

There are 3 push-buttons on the platform, which perform typical Android device behavior.

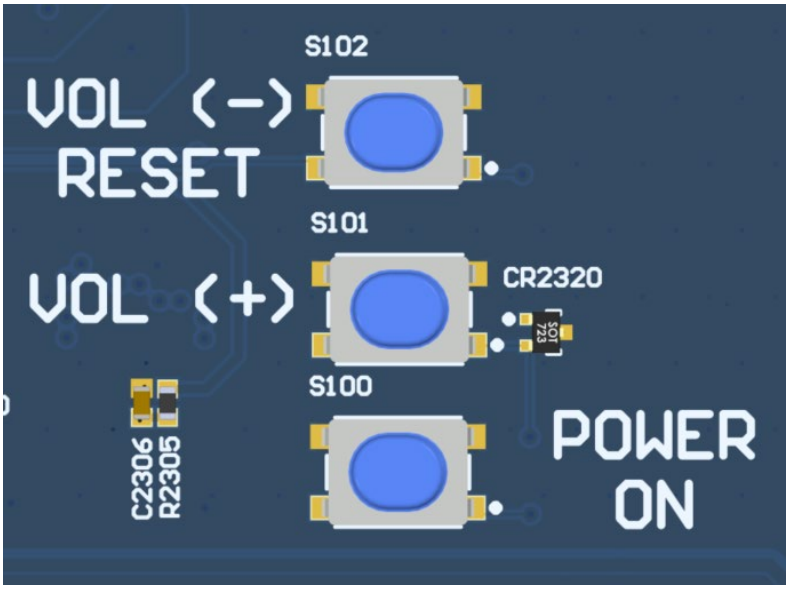

Figure 25 Buttons

- S100 – Power Button. Used to boot device, lock/wake device (Note the platform will auto-boot when power is applied when DIP SW S1 position 1 is set to 'ON').
- S101 – Volume Up
- S100 – Volume Down / Reset

3.8.23 USB Type C Port J2500

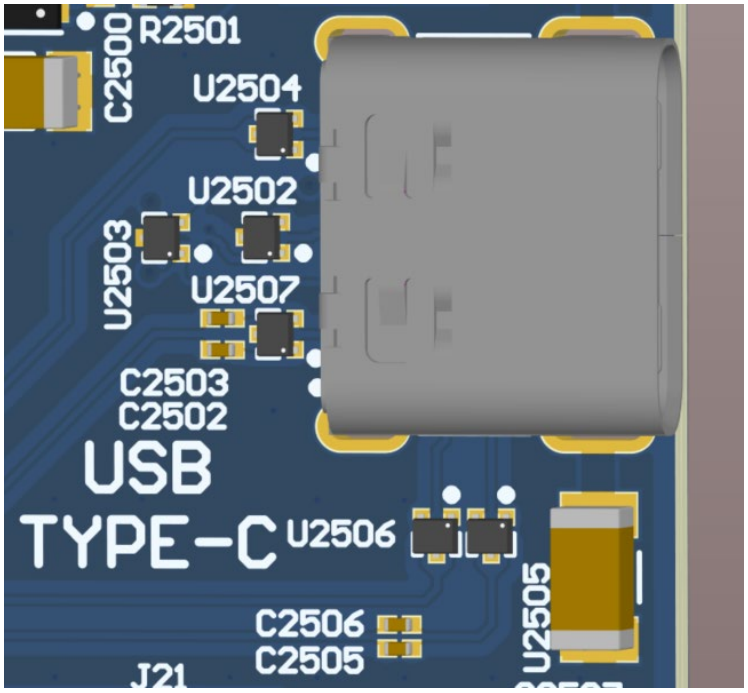

Figure 26 USB Type C Port J2500

J2500 is a USB 3.0 Type C Connector with SuperSpeed and High-Speed connections. The connector pinout follows the industry standard for USB 3.0. Embedded Display Port (eDP) is not supported.

Android ADB Access is possible on the HS lines using a USB Type C to Micro B adaptor.

3.8.24 LEDs

LED DS1 is connected to the PMI8952 ‘CHG_LED’ pin and signals charging status. It is configured by default to indicate battery charging status.

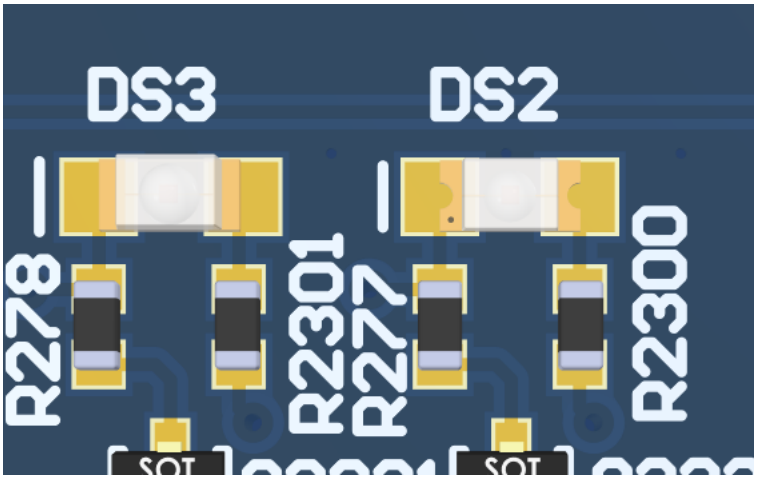

Figure 27 User LEDs

Two user controlled general purpose LED’s are also available:

- DS2 (BLUE) – Controlled by PMI_MPP_4_BLUE_LED_DRV
- DS3 (GREEN) – Controlled by PMI_MPP_2_GREEN_LED_DRV

Note that LED DS2320 is not supported with the 642A SOM.

3.8.25 HDMI Connector J25

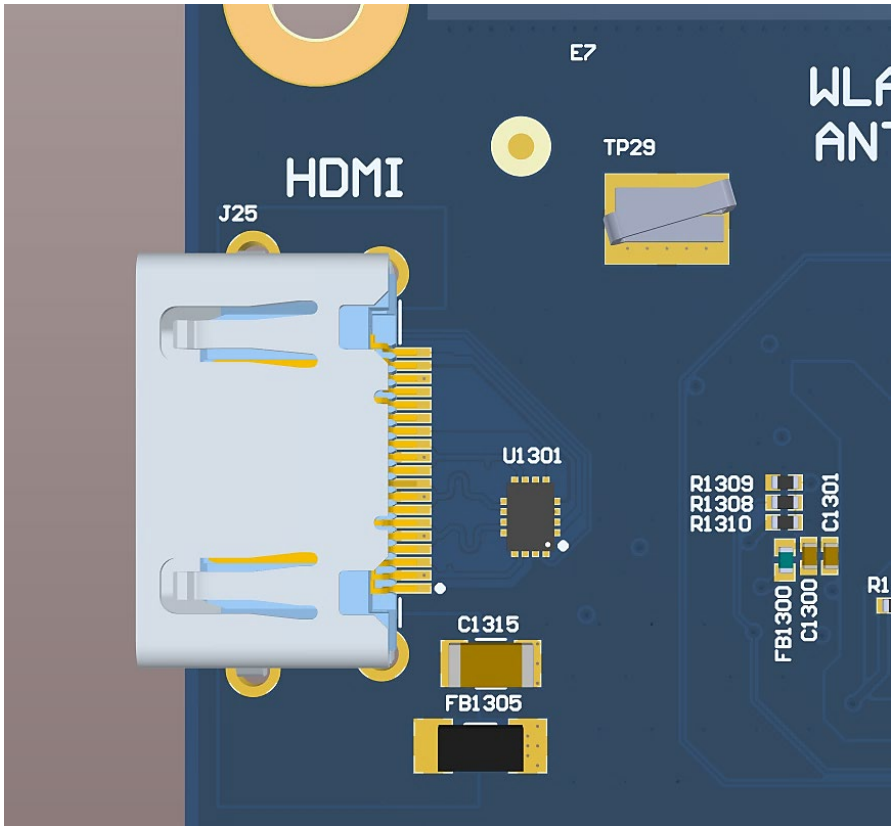

Figure 28 HDMI Connector J25

The on-board HDMI type A connector enables the Open-Q 624A development kit to connect to an external HDMI monitor/ television via an HDMI cable. The Open-Q 624A supports up to 1080P 60fps. Note that the HDMI port is for evaluation purposes only and may not be HDMI compliant.

3.9 Accessories

3.9.1 Camera Module Accessory

Two different camera modules are available as optional accessories and are not included in the development kit. They are available for purchase from the Lantronix online store in the Accessories section:

https://shop.intrinsyc.com/

1. 13MP Camera – based on the Sony IMX214 13MP sensor with a raw RGB MIPI CSI output, it interfaces to the development kit through the included 21cm JAE interface cable at connector. The camera can be connected to connectors J4 or J5 on the development kit.

Figure 29 - 13MP Camera Accessory

3.9.2 LCD / Touchscreen Accessory

An optional LCD/touchscreen display is available and can be connected to the Open-Q 624A development kit. The LCD can be used for the Android UI instead of the HDMI output, but both cannot be used at the same time. The LCD connects via the display connector J2, on the bottom of the carrier board. Connection is made with a 51-signal flex cable from JAE (JF08 series), which is included with the LCD accessory.

The compatible display accessory is called Open-Q 2100 LCD and is available for purchase on the Lantronix store: http://shop.intrinsyc.com.

Figure 30 LCD / Touchscreen Display Accessory

Resolution: 480x854

LCD Type: IPS

Touch: PCAP touch panel with cover glass

No of Lanes: 1 x 2 lane MIPI DSI interface via Display Board.

Diagonal Sizes: 4.5”

NOTE: The Open-Q 624A Development Kit has an HDMI video output and can be purchased with or without the optional LCD / touch panel. The development kit is shipped with the display output configured for HDMI 1080p as the default.
If you purchased the optional LCD display use the following ADB commands to configure the dev kit for use with the LCD.

```
adb reboot bootloader

fastboot oem select-display-panel

fastboot reboot
```

NOTE: these settings are persistent and retain the behavior after power cycles or reboots.
If you wish to change the display back to the HDMI output, use the following ADB commands:

```
adb reboot bootloader

for 720p resolution:  fastboot oem select-display-panel adv7533_720p

for 1080p resolution:  fastboot oem select-display-panel adv7533_1080p
```