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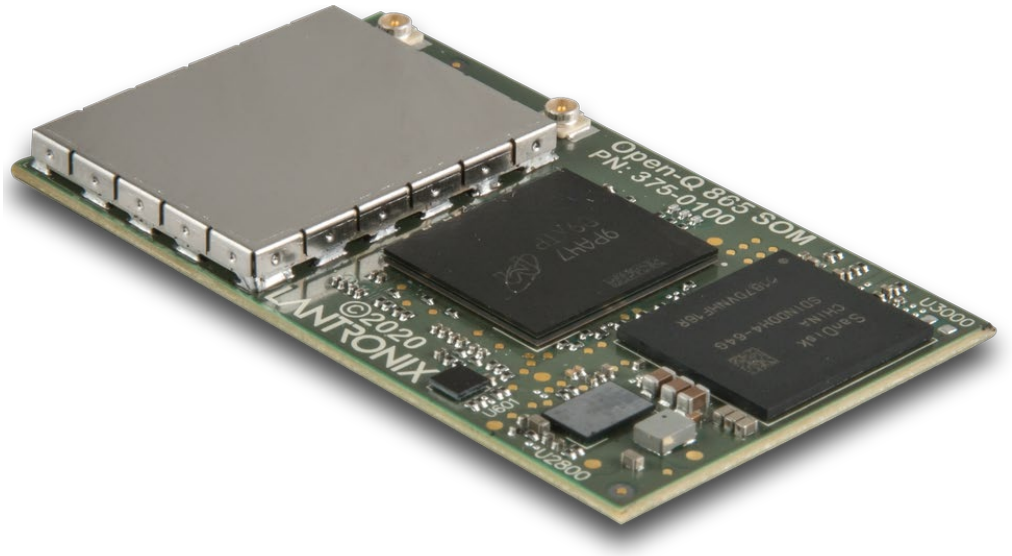

Open-Q™ 8250CS SOM
Hardware Datasheet

Part Number PDS-0024
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Revision History

Date	Rev.	Comments
February 2022	A	Initial Lantronix document.

For the latest revision of this product document, please go to: http://tech.intrinsyc.com.

Table of Contents

1 Introduction

This document applies to the Open-Q 8250CS SOM. Technical specifications for other SOMs in the Lantronix product line are covered under separate documents.

1.1 Purpose

The purpose of this document is to provide the technical specifications of the **Error! Unknown document property name.** Open-Q 8250CS SOM.

1.2 Scope

This document covers the following information on the Open-Q 8250CS SOM:

- Electrical and mechanical specifications
- SOM pinout
- Device handling and packaging
- Ordering information

1.3 Intended Audience

This document is intended for users who wish to understand the technical specifications of the Lantronix Open-Q 8250CS SOM.

1.4 Acronyms and Abbreviations

Acronym / Abbreviation	Definition
ANT	ANTenna
BAT, BATT	BATTery
BAM	Bus Access Manager
BLSP	BAM-based Low-Speed Peripheral
BOM	Bill of Materials
BT	Blue Tooth
CLK	Clock
CPU	Central Processing Unit
CS	Chip Select
CSI	Camera Serial Interface
DSI	Display Serial Interface
EMI	Electro-Magnetic Interference
EN	Enable
ERM	Eccentric Rotating Mass
ESD	Electro-Static Discharge
GND	GrouND
GPIO	General Purpose I/O
GPS	Global Positioning System

Acronym / Abbreviation	Definition
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
INT	INTerrupt
JTAG	Joint Test Action Group
LDO	Low Drop-Out
LRM	Linear Resonant Actuator
LTE	Long-Term Evolution
LPI	Low Power Island
MDP	Mobile Display Port
MI2S	Mobile Inter-IC Sound
MIC	MICrophone
MIPI	Mobile Industry Processor Interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
PCB	Printed Circuit Board
PCIE	Peripheral Component Interconnect Express
PWM	Pulse-Width Modulation
QUP	Qualcomm Universal Peripheral
RF	Radio Frequency
RX	Receive
SCL	Serial Clock
SDA	Serial Data
SDC	Secure Digital Interface
SOM	System on Module
SPI	Serial Peripheral Interface
SSC	Sensor Core
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UIM	User Interface Module
USB	Universal Serial Bus
WLAN	Wireless Local Area Network

1.5 Signal Name Suffix

Suffix	Definition
_N	Indicates that the signal is ACTIVE LOW
_P/N	Identifies the two signals comprising a differential pair

2 Documents

This section lists any parent and supplementary documents for the Open-Q 8250CS SOM Datasheet. Unless stated otherwise, applicable documents supersede this document and reference documents provide background and supplementary information.

2.1 Applicable Documents

Reference	Author	Title
A-1	Lantronix	Lantronix Purchase and Software License Agreement for the Open-Q 8250CS SOM

2.2 Reference Documents

Available at http://tech.intrinsyc.com (dev kit registration required).

Reference	Title
R-1	Open-Q 8250CS SOM Development Kit – User Guide
R-2	Open-Q 865 SOM – Carrier Board Design Guide
R-3	Open-Q 865 SOM Schematics (SOM and Carrier)
R-4	Open-Q 865 SOM Modular Certification OEM Integrator Guide

3 Summary of Features

The Open-Q 8250CS SOM contains the core of the Qualcomm QCS8250 architecture. Measuring 50mm x 29mm, the SOM is where all the processing occurs. It connects to a carrier board via three Hirose DF40 connectors totaling 320 pins, which allows essential power rails and signals to be exposed for supporting peripherals and interfaces on the platform.

3.1 SOM Block Diagram

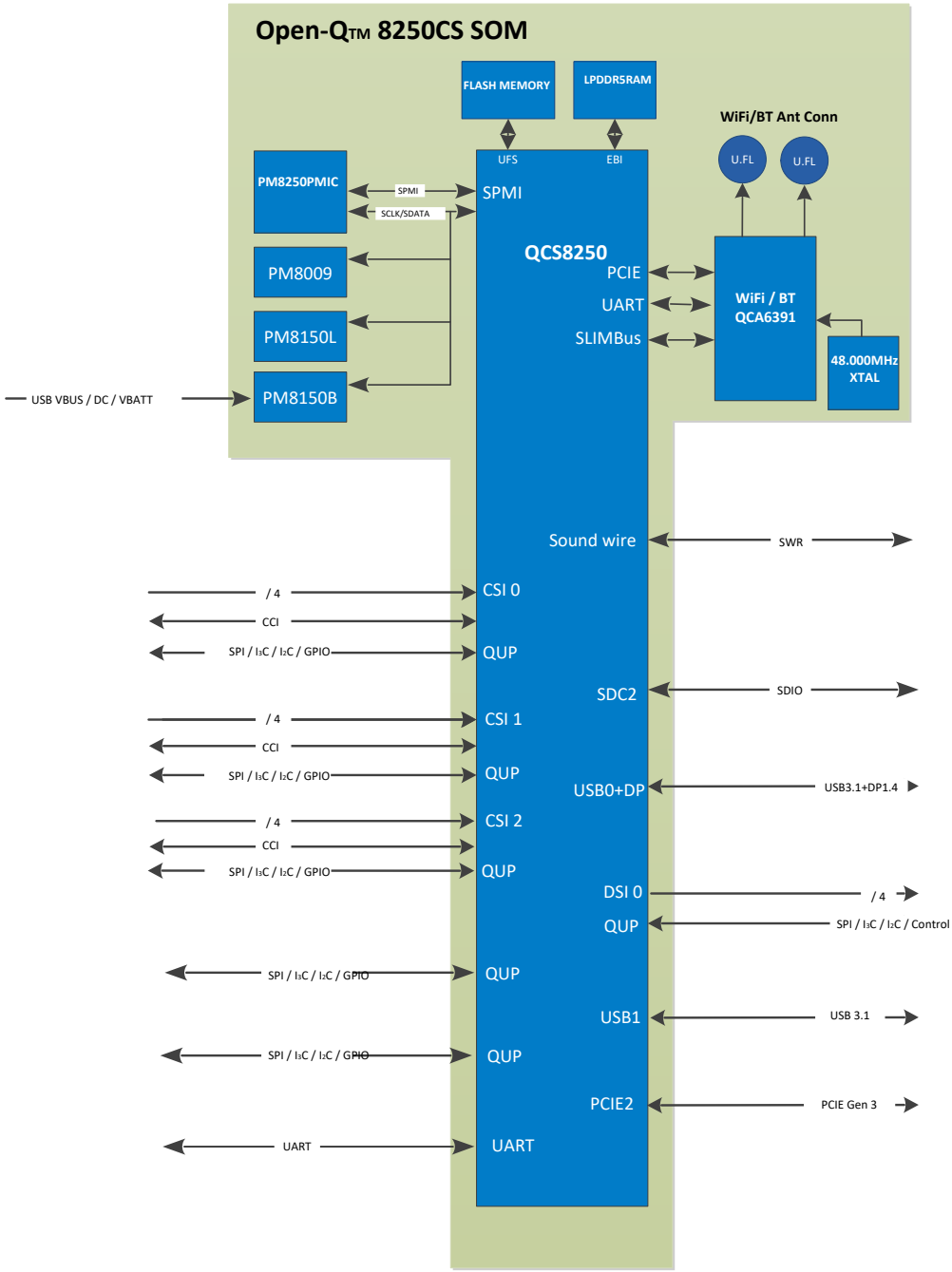

Figure 1. Open-Q 8250CS SOM Block Diagram

3.2 SOM Technical Specifications

See Table 1 for the Open-Q 8250CS SOM technical specifications.

Table 1. Open-Q 8250CS SOM Technical Specifications

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	QCS8250 CPU	Qualcomm QCS8250 Processors	One Qualcomm® Kryo™ Gold prime core with a 512 KB L2 cache, 2.842 GHz
			Three Qualcomm® Kryo™ Gold cores with a 256 KB L2 cache per core, 2.419 GHz
			Quad Low-Power Qualcomm® Kryo™ Silver cores with a 128 KB L2 cache per core, 1.805 GHz
	PM8250 PMIC and PM8150L PMIC	Qualcomm master PMIC for QCS8250 Processor	Power management, general housekeeping, user interface, and IC level interface support
	PM8150B PMIC	Qualcomm PMIC for QCS8250 Processor	Input power management, battery charging, battery management and general housekeeping
	PM8009 PMIC	Qualcomm Companion PMIC for QCS8250 Processor	Peripheral power management, general housekeeping
Memory	SDRAM Memory	4 Channel PoP LPDDR5 memory	4x 16-bit LPDDR5 SDRAM, 2750 MHz
	Flash Memory	Minimum 64GB UFS	UFS 2.1, 2x lane
Connectivity	Wi-Fi 5Ghz/2.4GHz	Qualcomm QCA6391 WLAN / Bluetooth Wireless Connectivity IC	2x2 MIMO WLAN compliant with IEEE802.11 a/b/g/n/ac/ax
	Bluetooth 2.4 GHz	Qualcomm QCA6391 WLAN / Bluetooth Wireless Connectivity IC	Compliant with Bluetooth version 5.0
RF Interfaces (see Section 4.3)	WLAN / BT	2 antenna connectors on SOM for 2x2 MIMO Wi-Fi. Bluetooth uses one of the 2 antenna ports.	2 x U.FL, 50 ohm coaxial connectors
Audio Interfaces	Digital MI2S	Two MI2S ports	Two 2-lane MI2S ports
	SoundWire	One SoundWire interface	Two Tx and two Rx data lines; with optional configurations for three Tx and one Rx data lines

Subsystem / Connectors	Feature Set	Description	Specification
Digital Interfaces	MIPI CSI	Three 4-lane MIPI CSI Camera interfaces	4-lane supporting (4/4/4) D-PHY 1.2 (2.5 Gbps / lane) Up to 64 MP 30fps with a dual ISP
	MIPI DSI	Two 4-lane MIPI DSI Display interfaces	Supporting D-PHY 1.2 (2.5 Gbps / lane) and 4K60
	USB	Two USB 3.1 Ports	One USB 3.1 Type-C with support for DisplayPort 1.4 One USB 3.1 Type-A
	PCIe	PCIe Gen 3	2-lane Gen 3 with PHY 3.0
	SDIO	One 4-bit Secure Digital interface	SD v3.0, dual voltage interface
	GPIO / I2C / I3C / SPI / UART	Configurable IO	Configurable IO exposed as GPIO or QUP ports, giving GPIO, I2C, I3C, SPI, and UART connections options.
Connectors	1x 120-pin board to board connectors 2x 100-pin board to board connector	1x Hirose 120-pin DF40C-120DP header connectors 2x Hirose 100-pin DF40C-100DP header connectors	320 pins total for connection to carrier board

4 I/O Definitions

4.1 Location of Major Components

Figure 2 and Figure 3 identify the major components and connectors found on the top and bottom of the Open-Q 8250CS SOM.

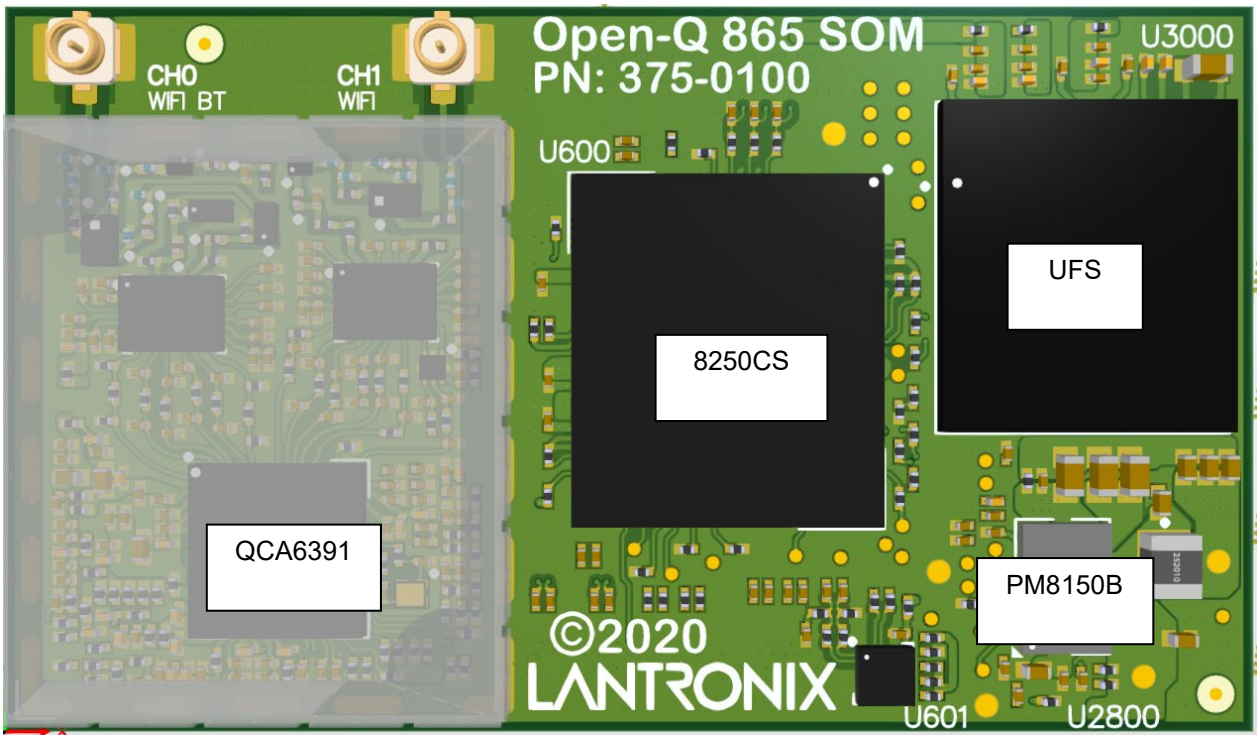

Figure 2. Open-Q 8250CS SOM Top View

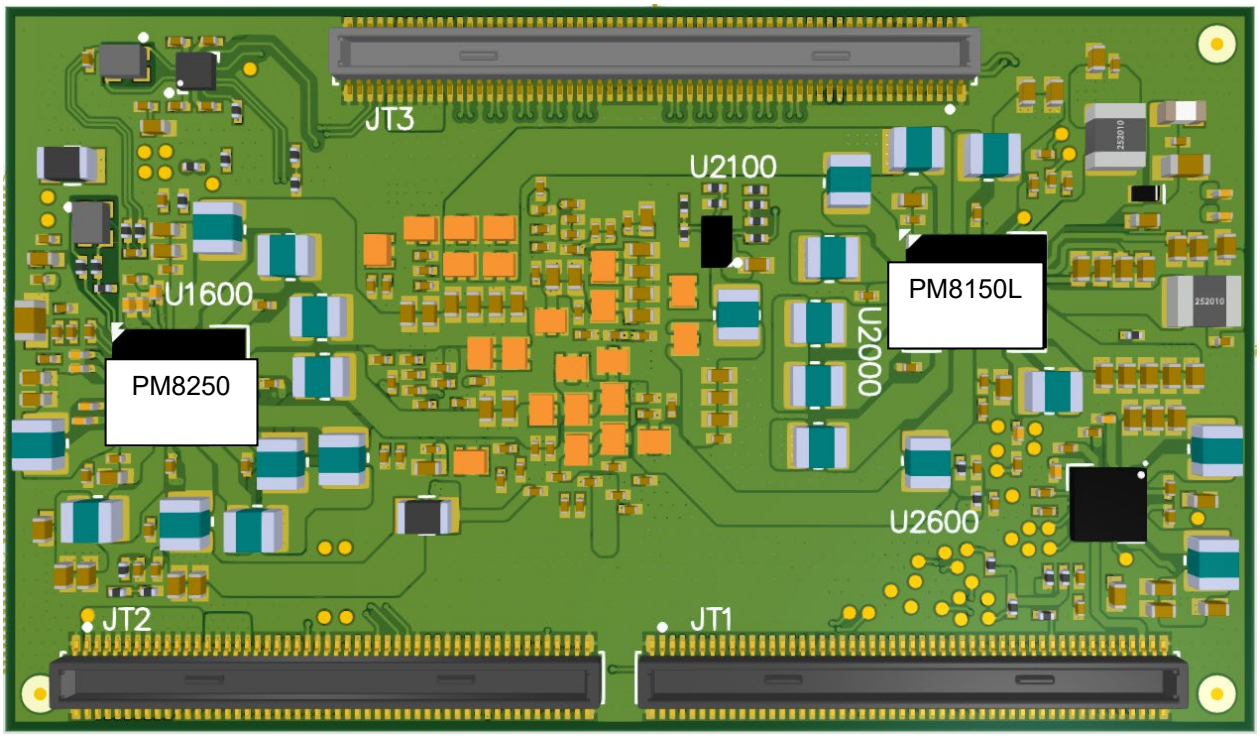

Figure 3. Open-Q 8250CS SOM Bottom View

The SOM mating connectors JT1, JT2, and JT3 are located on the bottom side of the SOM. The connector pin 1 locations are shown in Figure 4 (looking at bottom of SOM). Key dimensions are provided in Section 6.

The JT1 and JT2 connectors are Hirose DF40C-100DP-0.4V. The JT3 connector is Hirose DF40C-120DP-0.4V.

See Section 6.3 for information on the available mating connectors.

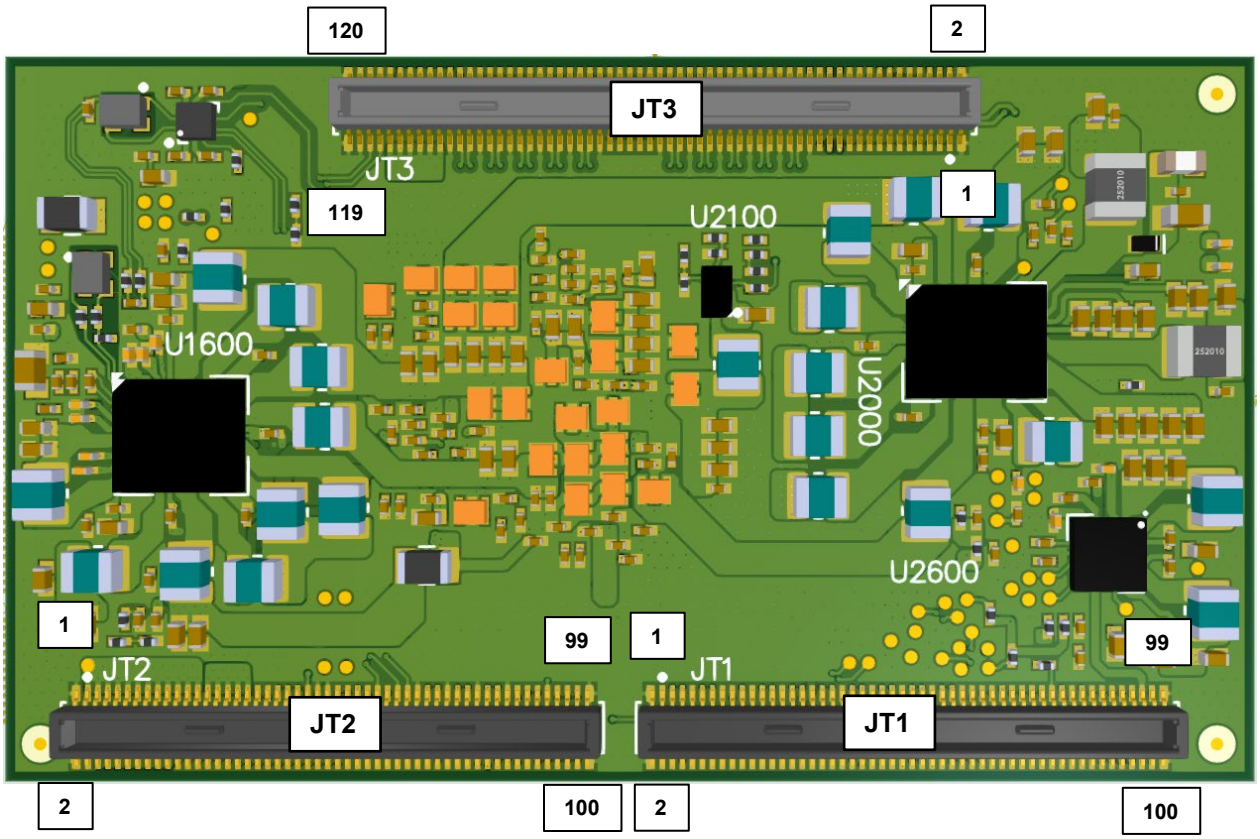

Figure 4. Pin Locations of Board-to-Board Connectors

4.2 Board to Board Connector Signal Assignments

Table 2, Table 3, and Table 4 list the pinouts of the three Open-Q 8250CS SOM board-to-board (B2B) connectors JT1, JT2, and JT3 respectively. For more information on how to use these signals in a Carrier Board design, see the SOM Carrier Board Design Guide (Reference Document R-2).

***Note**: The SOM schematic (Reference Document R-3) is the controlling document. In the event of pinout difference(s) between this document and the SOM schematic, the SOM schematic shall take precedence.*

Table 2. B2B Connector JT1 Pinouts

Pin #	JT1 Signal Name	Description
1	GND	Ground reference for the SOM
2	GND	Ground reference for the SOM
3	MIPI_DSI0_LANE3_N	MIPI display serial interface 0 data
4	GPIO_0_GNSS_IRQ	Configurable GPIO
5	MIPI_DSI0_LANE3_P	MIPI display serial interface 0 data
6	PM8250_GPIO3_M2_SLEEP_CLK	PCIE Control Signal / Configurable GPIO
7	GND	Ground reference for the SOM
8	GND	Ground reference for the SOM

Pin #	JT1 Signal Name	Description
9	MIPI_DSI0_LANE1_N	MIPI display serial interface 0 data
10	PCIE2_RX1_N	PCIE Gen3 Port 2 – receive data
11	MIPI_DSI0_LANE1_P	MIPI display serial interface 0 data
12	PCIE2_RX1_P	PCIE Gen3 Port 2 – receive data
13	GND	Ground reference for the SOM
14	GND	Ground reference for the SOM
15	MIPI_DSI0_LANE0_N	MIPI display serial interface 0 data
16	PCIE2_TX0_N	PCIE Gen3 Port 2 – transmit data
17	MIPI_DSI0_LANE0_P	MIPI display serial interface 0 data
18	PCIE2_TX0_P	PCIE Gen3 Port 2 – transmit data
19	GND	Ground reference for the SOM
20	GND	Ground reference for the SOM
21	MIPI_DSI0_CLK_N	MIPI display serial interface 0 clock
22	PCIE2_TX1_N	PCIE Gen3 Port 2 – transmit data
23	MIPI_DSI0_CLK_P	MIPI display serial interface 0 clock
24	PCIE2_TX1_P	PCIE Gen3 Port 2 – transmit data
25	GND	Ground reference for the SOM
26	GND	Ground reference for the SOM
27	MIPI_DSI0_LANE2_N	MIPI display serial interface 0 data
28	PCIE2_REFCLK_P	PCIE Gen3 Port 2 – reference clock
29	MIPI_DSI0_LANE2_P	MIPI display serial interface 0 data
30	PCIE2_REFCLK_N	PCIE Gen3 Port 2 – reference clock
31	GND	Ground reference for the SOM
32	GND	Ground reference for the SOM
33	MIPI_DSI1_LANE1_N	MIPI display serial interface 1 data
34	PCIE2_RX0_N	PCIE Gen3 Port 2 – receive data
35	MIPI_DSI1_LANE1_P	MIPI display serial interface 1 data
36	PCIE2_RX0_P	PCIE Gen3 Port 2 – receive data
37	GND	Ground reference for the SOM
38	GND	Ground reference for the SOM
39	MIPI_DSI1_LANE0_N	MIPI display serial interface 1 data
40	USB1_SS_RX_N	USB Type A port – SuperSpeed Receive Data
41	MIPI_DSI1_LANE0_P	MIPI display serial interface 1 data
42	USB1_SS_RX_P	USB Type A port – SuperSpeed Receive Data
43	GND	Ground reference for the SOM
44	GND	Ground reference for the SOM
45	MIPI_DSI1_CLK_N	MIPI display serial interface 1 clock
46	USB1_HS_D_N	USB Type A port – High Speed Data
47	MIPI_DSI1_CLK_P	MIPI display serial interface 1 clock
48	USB1_HS_D_P	USB Type A port – High Speed Data

Pin #	JT1 Signal Name	Description
49	GND	Ground reference for the SOM
50	GND	Ground reference for the SOM
51	MIPI_DSI1_LANE2_N	MIPI display serial interface 1 data
52	USB1_SS_TX_P	USB Type A port – SuperSpeed Transmit Data
53	MIPI_DSI1_LANE2_P	MIPI display serial interface 1 data
54	USB1_SS_TX_N	USB Type A port – SuperSpeed Transmit Data
55	GND	Ground reference for the SOM
56	GND	Ground reference for the SOM
57	MIPI_DSI1_LANE3_P	MIPI display serial interface 1 data
58	GPIO_98_CAM1_STANDBY	Camera standby output 1 / Configurable GPIO
59	MIPI_DSI1_LANE3_N	MIPI display serial interface 1 data
60	GPIO_94_CAM_MCLK0	Camera master clock 0 / Configurable GPIO
61	GND	Ground reference for the SOM.
62	GPIO_95_CAM_MCLK1	Camera master clock 1 / Configurable GPIO
63	GPIO_117_QUP2_CAM_SPI2_CLK	QUP2 SPI, UART / Configurable GPIO
64	PM8250_GPIO6_KYPD_VOLP_N	Volume Up Button / Configurable GPIO
65	GPIO_146_WCD_SWR_TX_CLK	Audio Soundwire Transmit, MI2S / Configurable GPIO
66	CBL_PWR_N	Optional input that, when grounded, can initiate an auto power on sequence
67	GPIO_147_WCD_SWR_TX_DATA0	Audio Soundwire Transmit, MI2S / Configurable GPIO
68	GPIO_102_CCI_I2C_SCL0	Camera control interface 0 I2C / Configurable GPIO
69	GPIO_148_WCD_SWR_TX_DATA1	Audio Soundwire Transmit, MI2S / Configurable GPIO
70	GPIO_101_CCI_I2C_SDA0	Camera control interface 0 I2C / Configurable GPIO
71	GPIO_154_LPI_MI2S1_DATA0	Audio DMIC, MI2S / Configurable GPIO
72	GPIO_96_CAM_MCLK2	Camera master clock 2 / Configurable GPIO
73	GPIO_153_LPI_MI2S1_WS	Audio DMIC, MI2S / Configurable GPIO
74	GPIO_89_W_DISABLE_N	PCIE Control Signal / Configurable GPIO
75	GPIO_155_LPI_MI2S1_DATA1	Audio DMIC, MI2S / Configurable GPIO
76	GPIO_114_CAM6_RST_N	Configurable GPIO
77	GPIO_152_LPI_MI2S1_CLK	Audio DMIC, MI2S / Configurable GPIO
78	GPIO_104_CCI_I2C_SCL1	Camera control interface 1 I2C / Configurable GPIO
79	RESIN_VOLDN_N	Reset Input / Volume Down Button

Pin #	JT1 Signal Name	Description
80	GPIO_103_CCI_I2C_SDA1	Camera control interface 1 I2C / Configurable GPIO
81	GPIO_149_WCD_SWR_RX_CLK	Audio Soundwire Receive, MI2S / Configurable GPIO
82	GPIO_42_QUP14_FP_SPI_CLK	QUP14 SPI, UART / Configurable GPIO
83	GPIO_150_WCD_SWR_RX_DATA 0	Audio Soundwire Receive, MI2S / Configurable GPIO
84	GPIO_40_QUP14_FP_SPI_MISO	QUP14 SPI, UART, I2C, I3C / Configurable GPIO
85	GPIO_151_WCD_SWR_RX_DATA 1	Audio Soundwire Receive, MI2S / Configurable GPIO
86	GPIO_41_QUP14_FP_SPI_MOSI	QUP14 SPI, UART, I2C, I3C / Configurable GPIO
87	GPIO_10_QUP4_CAM_SPI1_CLK	QUP4 SPI, UART / Configurable GPIO
88	GPIO_43_QUP14_FP_SPI_CS	QUP14 SPI, UART / Configurable GPIO
89	GPIO_11_QUP4_CAM_SPI1_CS0_ N	QUP4 SPI, UART / Configurable GPIO
90	SDR_GRFC2	PCIE wireless coexistence control
91	GPIO_9_QUP4_CAM_SPI1_MOSI	QUP4 SPI, UART, I2C / Configurable GPIO
92	HST_WL_TX_EN	PCIE wireless coexistence control
93	GPIO_8_QUP4_CAM_SPI1_MISO	QUP4 SPI, UART, I2C / Configurable GPIO
94	VREG_S4A_1P8	PM8250 PMIC +1.8V SMPS Output typically used for general IOVCC. 600mA capacity is expected.
95	VREG_L8C_1P8	PM8150L PMIC +1.8V LDO Output typically used for Sensor IOVCC. 150mA capacity is expected.
96	VREG_S4A_1P8	See JT1 pin 94
97	VREG_L7F_1P8	PM8009 PMIC +1.8V LDO output typically used for camera IOVCC. 300mA capacity is expected.
98	VREG_L5F_2P85	PM8009 PMIC +2.85V LDO output typically used for camera AVDD. 300mA capacity is expected.
99	PM8150L_GP10_PWM	PMIC Configurable GPIO
100	VREG_L11C_3P3	PM8150L PMIC +1.8V LDO Output typically used for display / touch AVDD. 300mA capacity is expected.

Table 3. B2B Connector JT2 Pinouts

Pin #	JT2 Signal Name	Description
1	SOM_SYS_PWR	Main power source for SOM. Single cell Lithium battery connection or 3.8V DC power input.
2	GND	Ground reference for the SOM.
3	SOM_SYS_PWR	See JT2 pin 1
4	SOM_SYS_PWR	See JT2 pin 1
5	SOM_SYS_PWR	See JT2 pin 1
6	SOM_SYS_PWR	See JT2 pin 1
7	SOM_SYS_PWR	See JT2 pin 1
8	SOM_SYS_PWR	See JT2 pin 1
9	SOM_SYS_PWR	See JT2 pin 1
10	SOM_SYS_PWR	See JT2 pin 1
11	SOM_SYS_PWR	See JT2 pin 1
12	SOM_SYS_PWR	See JT2 pin 1
13	SOM_SYS_PWR	See JT2 pin 1
14	SOM_SYS_PWR	See JT2 pin 1
15	SOM_SYS_PWR	See JT2 pin 1
16	SOM_SYS_PWR	See JT2 pin 1
17	SOM_SYS_PWR	See JT2 pin 1
18	SOM_SYS_PWR	See JT2 pin 1
19	SOM_SYS_PWR	See JT2 pin 1
20	BATT_ID	Battery identification input that can be used for missing battery detection and charger enable / disable
21	SOM_SYS_PWR	See JT2 pin 1
22	VBATT_CONN_VSENSE_N	Battery voltage sense input
23	SOM_SYS_PWR	See JT2 pin 1
24	VBATT_CONN_VSENSE_P	Battery voltage sense input
25	USB_VBUS	USB Type-C VBUS connection. When used as power input, this is the charge power source for battery powered applications. For USB host mode applications, this is a power output.
26	SKIN_THERM	Auxiliary temperature input to PMIC ADC typically connected to remote thermistor located in ‘quiet’ area of carrier board
27	USB_VBUS	See JT2 pin 25
28	BATT_THERM	Battery thermistor input used for measuring battery pack temperature for safe charger operation
29	USB_VBUS	See JT2 pin 25

Pin #	JT2 Signal Name	Description
30	PHONE_ON_N	Input typically connected to keypad power-on button that, when grounded, can initiate a power on sequence or reset
31	USB_VBUS	See JT2 pin 25
32	GPIO_66_MDP_VSYNC_P	Display vertical sync / Configurable GPIO
33	USB_VBUS	See JT2 pin 25
34	GPIO_67_DISPLAY_ID	Configurable GPIO
35	USB_CC2	USB Type C port – CC2 pin
36	GPIO_144_BL0_EN	Configurable GPIO
37	USB_CC1	USB Type C port – CC1 pin
38	GPIO_78_CAM2_RST_N	Camera 2 reset output / Configurable GPIO
39	RGB_BLUE	RGB LED high-side current source
40	PM8150L_GP06_LCD_PWM	PMIC Configurable GPIO
41	RGB_GREEN	RGB LED high-side current source
42	GPIO_127_WSA1_EN	Configurable GPIO
43	RGB_RED	RGB LED high-side current source
44	GPIO_77_SD_UFS_CARD_DET_N	SD Card Detect Input / Configurable GPIO
45	GPIO_112_IMU2_INT	Sensor IRQ / Configurable GPIO
46	GPIO_115_QUP2_CAM_SPI2_MISO	QUP0 SPI, UART, I2C / Configurable GPIO
47	GND	Ground reference for the SOM.
48	GPIO_116_QUP2_CAM_SPI2_MOSI	QUP0 SPI, UART, I2C / Configurable GPIO
49	GND	Ground reference for the SOM
50	GPIO_169_SNS_I2C3_SCL	SSC I/O 9
51	GPIO_26_USB_VBUS_EN	Configurable GPIO
52	GPIO_168_SNS_I2C3_SDA	SSC I/O 8
53	GPIO_75_DISP0_RESET_N	Display Reset Output / Configurable GPIO
54	GND	Ground reference for the SOM
55	GPIO_93_CAM0_RST_N	Camera 0 Reset Output / Configurable GPIO
56	USB0_SS_TX1_N	USB Type C port – SuperSpeed Transmit Data
57	GPIO_3_HDMI_3P3_EN	Configurable GPIO
58	USB0_SS_TX1_P	USB Type C port – SuperSpeed Transmit Data
59	GPIO_27_BOOTCFG_1	Boot Configuration Input / Configurable GPIO
60	GND	Ground reference for the SOM
61	GPIO_2_HDMI_RSTN	Configurable GPIO

Pin #	JT2 Signal Name	Description
62	USB0_SS_RX1_P	USB Type C port – SuperSpeed Receive Data
63	GPIO_132_FORCE_USB_BOOT	Boot Configuration Input / Configurable GPIO
64	USB0_SS_RX1_N	USB Type C port – SuperSpeed Receive Data
65	GPIO_1_HDMI_INT	Configurable GPIO
66	GND	Ground reference for the SOM
67	GND	Ground reference for the SOM
68	USB_SBU_P	USB Type C port – Sideband / DisplayPort auxiliary channel
69	USB0_HS_D_P	USB Type C port – High Speed Data
70	USB_SBU_N	USB Type C port – Sideband / DisplayPort auxiliary channel
71	USB0_HS_D_N	USB Type C port – High Speed Data
72	GPIO_133_MI2S2_I2S_SCK	Audio MI2S / Configurable GPIO
73	GND	Ground reference for the SOM
74	GPIO_135_MI2S2_I2S_WS	Audio MI2S / Configurable GPIO
75	USB0_SS_RX0_N	USB Type C port – SuperSpeed Receive Data
76	GPIO_137_MI2S2_I2S_DAT1	Audio MI2S / Configurable GPIO
77	USB0_SS_RX0_P	USB Type C port – SuperSpeed Receive Data
78	GPIO_134_MI2S2_I2S_DAT0	Audio MI2S / Configurable GPIO
79	GND	Ground reference for the SOM
80	GPIO_170_SNS_I2C4_SDA	SSC I/O 10
81	USB0_SS_TX0_N	USB Type C port – SuperSpeed Transmit Data
82	GPIO_171_SNS_I2C4_SCL	SSC I/O 11
83	USB0_SS_TX0_P	USB Type C port – SuperSpeed Transmit Data
84	GPIO_159_LPI_MI2S2_DATA1	Audio DMIC, MI2S / Configurable GPIO
85	GND	Ground reference for the SOM
86	GPIO_158_LPI_MI2S2_DATA0	Audio DMIC, MI2S / Configurable GPIO
87	GPIO_34_QUP12_2_DEBUG_UART_TX	QUP12 UART / Configurable GPIO
88	GPIO_156_WSA_SWR_CLK	Audio Soundwire, MI2S / Configurable GPIO
89	GPIO_35_QUP12_3_DEBUG_UART_RX	QUP12 UART / Configurable GPIO
90	GPIO_157_WSA_SWR_DATA	Audio Soundwire, MI2S / Configurable GPIO
91	GPIO_64_SAR_INT_N	Sensor IRQ / Configurable GPIO

Pin #	JT2 Signal Name	Description
92	GPIO_32_WCD_RESET_N	Audio Codec Reset output / Configurable GPIO
93	GPIO_164_SNS_SPI2_MISO	SSC I/O 4
94	GPIO_118_QUP2_CAM_SPI2_CS0_N	QUP0 SPI, UART / Configurable GPIO
95	GPIO_165_SNS_SPI2_MOSI	SSC I/O 5
96	GPIO_85_PCIE2_RST_N	PCIE Control Signal / Configurable GPIO
97	GPIO_166_SNS_SPI2_CLK	SSC I/O 6
98	GPIO_86_PCIE2_CLK_REQ_N	PCIE Control Signal / Configurable GPIO
99	GPIO_167_SNS_SPI2_CS0_N	SSC I/O 7
100	GPIO_87_PCIE2_WAKE_N	PCIE Control Signal / Configurable GPIO

Table 4. B2B Connector JT3 Pinouts

Pin #	JT3 Signal Name	Description
1	VREG_L13A_3P0	PM8250 PMIC +3.0V LDO Output option for display / touch AVDD. 150mA capacity is expected.
2	VREG_L9C_2P96	PM8150L PMIC +2.96V LDO Output typically used for uSD card VDD. 600mA capacity is expected.
3	GPIO_128_WSA2_EN	Configurable GPIO
4	VREG_L9C_2P96	See JT3 pin 2
5	GPIO_97_CAM0_STANDBY	Camera standby output 0 / Configurable GPIO
6	VREG_L9C_2P96	See JT3 pin 2
7	GPIO_129_PRESS_INT	Sensor IRQ / Configurable GPIO
8	GPIO_4_QUP1_NFC_I2C_SDA	QUP1 I2C, I3C / Configurable GPIO
9	GPIO_161_SNS_I3C0_SCL	SSC I/O 1
10	GPIO_5_QUP1_NFC_I2C_SCL	QUP1 I2C, I3C / Configurable GPIO
11	GPIO_160_SNS_I3C0_SDA	SSC I/O 0
12	CABC	Display PWM input for backlight brightness control
13	GPIO_36_QUP13_TS_I2C_SDA	QUP13 SPI, UART, I2C / Configurable GPIO
14	VREG_L10C_3P0	PM8150L PMIC +3.0V LDO Output typically used for Sensor AVDD. 600mA capacity is expected.
15	GPIO_37_QUP13_TS_I2C_SCL	QUP13 SPI, UART, I2C / Configurable GPIO
16	VREG_L10C_3P0	See JT3 pin 14
17	PM_VCOIN	Optional +3V rechargeable coin cell backup battery connection to SOM
18	VREG_L14A_1P8	PM8250 PMIC +1.8V LDO Output typically used for display / touch IOVCC. 250mA capacity is expected.
19	GPIO_38_QUP13_TS_RESET_N	QUP13 SPI, UART / Configurable GPIO
20	VDISP_P_OUT	Display bias SMPS regulated output
21	GPIO_39_QUP13_TS_INT_N	QUP13 SPI, UART / Configurable GPIO
22	VDISP_M_OUT	Display bias SMPS regulated output
23	VREG_L1F_1P2	PM8009 PMIC +1.2V LDO Output typically used for camera DVDD. 500mA capacity is expected.
24	VREG_L2F_1P2	PM8009 PMIC +1.2V LDO Output typically used for camera DVDD. 500mA capacity is expected.
25	VREG_L1F_1P2	See JT3 pin 23
26	VREG_L2F_1P2	See JT3 pin 24
27	VREG_L3F_1P0	PM8009 PMIC +1.0V LDO Output typically used for camera DVDD. 250mA capacity is expected.
28	GPIO_92_CAM1_RST_N	Camera 1 reset output / Configurable GPIO
29	GND	Ground reference for the SOM

Pin #	JT3 Signal Name	Description
30	GPIO_123_IMU1_INT	Sensor IRQ / Configurable GPIO
31	MIPI_CSI2_LANE2_P	MIPI camera serial interface 2 data
32	GPIO_121_HALL_INT_N	Sensor IRQ / Configurable GPIO
33	MIPI_CSI2_LANE2_N	MIPI camera serial interface 2 data
34	GPIO_113_MAG_INT_N	Sensor IRQ / Configurable GPIO
35	GND	Ground reference for the SOM
36	GPIO_122_ALSP_INT_N	Sensor IRQ / Configurable GPIO
37	MIPI_CSI2_LANE1_P	MIPI camera serial interface 2 data
38	GND	Ground reference for the SOM
39	MIPI_CSI2_LANE1_N	MIPI camera serial interface 2 data
40	MIPI_CSI1_LANE2_P	MIPI camera serial interface 1 data
41	GND	Ground reference for the SOM
42	MIPI_CSI1_LANE2_N	MIPI camera serial interface 1 data
43	MIPI_CSI2_CLK_P	MIPI camera serial interface 2 clock
44	GND	Ground reference for the SOM
45	MIPI_CSI2_CLK_N	MIPI camera serial interface 2 clock
46	MIPI_CSI1_LANE1_P	MIPI camera serial interface 1 data
47	GND	Ground reference for the SOM
48	MIPI_CSI1_LANE1_N	MIPI camera serial interface 1 data
49	MIPI_CSI2_LANE0_P	MIPI camera serial interface 2 data
50	GND	Ground reference for the SOM
51	MIPI_CSI2_LANE0_N	MIPI camera serial interface 2 data
52	MIPI_CSI1_CLK_P	MIPI camera serial interface 1 clock
53	GND	Ground reference for the SOM
54	MIPI_CSI1_CLK_N	MIPI camera serial interface 1 clock
55	MIPI_CSI2_LANE3_P	MIPI camera serial interface 2 data
56	GND	Ground reference for the SOM
57	MIPI_CSI2_LANE3_N	MIPI camera serial interface 2 data
58	MIPI_CSI1_LANE0_P	MIPI camera serial interface 1 dat
59	GND	Ground reference for the SOM
60	MIPI_CSI1_LANE0_N	MIPI camera serial interface 1 data
61	GPIO_99_CAM2_STANDBY	Camera standby output 2 / Configurable GPIO
62	GND	Ground reference for the SOM
63	GPIO_58_QUP18_SPI_CLK	QUP18 SPI, UART / Configurable GPIO
64	MIPI_CSI1_LANE3_P	MIPI camera serial interface 1 data
65	GPIO_56_QUP18_SPI_MISO	QUP18 SPI, UART, I2C / Configurable GPIO
66	MIPI_CSI1_LANE3_N	MIPI camera serial interface 1 data
67	GPIO_57_QUP18_SPI_MOSI	QUP18 SPI, UART, I2C / Configurable GPIO
68	GND	Ground reference for the SOM
69	GPIO_59_QUP18_SPI_CS_N	QUP18 SPI, UART / Configurable GPIO

Pin #	JT3 Signal Name	Description
70	SDM_RESOUT_N	Processor reset output used for indicating power on sequence
71	GND	Ground reference for the SOM
72	WLAN_COEX_MDMUART_TX	PCIe wireless coexistence UART
73	MIPI_CSI0_LANE2_P	MIPI camera serial interface 0 data
74	WLAN_COEX_MDMUART_RX	PCIe wireless coexistence UART
75	MIPI_CSI0_LANE2_N	MIPI camera serial interface 0 data
76	VREG_WLED	Display backlight LED current supply output
77	GND	Ground reference for the SOM
78	WLED_SINK3	Display backlight LED current supply sink
79	MIPI_CSI0_LANE3_P	MIPI camera serial interface 0 data
80	WLED_SINK1	Display backlight LED current supply sink
81	MIPI_CSI0_LANE3_N	MIPI camera serial interface 0 data
82	WLED_SINK2	Display backlight LED current supply sink
83	GND	Ground reference for the SOM
84	GND	Ground reference for the SOM
85	MIPI_CSI0_LANE1_P	MIPI camera serial interface 0 data
86	SDC2_DATA0	Secure Digital IO data
87	MIPI_CSI0_LANE1_N	MIPI camera serial interface 0 data
88	SDC2_DATA1	Secure Digital IO data
89	GND	Ground reference for the SOM
90	SDC2_CLK	Secure Digital IO clock
91	MIPI_CSI0_LANE0_N	MIPI camera serial interface 0 data
92	SDC2_CMD	Secure Digital IO command
93	MIPI_CSI0_LANE0_P	MIPI camera serial interface 0 data
94	SDC2_DATA2	Secure Digital IO data
95	GND	Ground reference for the SOM
96	SDC2_DATA3	Secure Digital IO data
97	MIPI_CSI0_CLK_N	MIPI camera serial interface 0 clock
98	GND	Ground reference for the SOM
99	MIPI_CSI0_CLK_P	MIPI camera serial interface 0 clock
100	PM8150L_GPI04_SPARE	PMIC Configurable GPIO
101	GND	Ground reference for the SOM
102	VPH_PWR	Main SOM System power output node. Follows the SOM_SYS_PWR Supply voltage level. Typically used for powering carrier board peripherals. 3000mA capacity is expected.
103	VPH_PWR	See JT3 pin 102
104	VPH_PWR	See JT3 pin 102
105	VPH_PWR	See JT3 pin 102
106	VPH_PWR	See JT3 pin 102

Pin #	JT3 Signal Name	Description
107	VPH_PWR	See JT3 pin 102
108	VPH_PWR	See JT3 pin 102
109	VPH_PWR	See JT3 pin 102
110	VPH_PWR	See JT3 pin 102
111	VPH_PWR	See JT3 pin 102
112	VPH_PWR	See JT3 pin 102
113	VPH_PWR	See JT3 pin 102
114	GPIO_15_RADAR_INT	Boot Status Indicator / Sensor IRQ / Configurable GPIO
115	GPIO_162_SNS_I3C1_SDA	SSC I/O 2
116	GND	Ground reference for the SOM
117	GPIO_163_SNS_I3C1_SCL	SSC I/O 3
118	GND	Ground reference for the SOM
119	GND	Ground reference for the SOM
120	GND	Ground reference for the SOM

4.3 RF Antenna Connections

The Open-Q 8250CS SOM provides Wi-Fi and Bluetooth connectivity via the Qualcomm QCA6391 chipset. This provides 802.11 a/b/g/n/ac/ax 2x2 MIMO, dual-band Wi-Fi, and Bluetooth 5.x. The 2x2 MIMO Wi-Fi requires two antennas for maximum throughput and operates at both 2.4GHz and 5GHz. Bluetooth uses only one of the antennas (CH0) and only operates at 2.4GHz. To support full performance of the Wi-Fi and Bluetooth, two dual-band antennas are required. If only Bluetooth is used, it can be supported with one single-band 2.4GHz antenna connected to the CH0 port.

For information on the recommended antennas to use with the SOM, see the regulatory certifications described in Section 9 and listed in Reference Document R-4.

The SOM uses two U.FL coaxial connectors (Hirose U.FL-R-SMT-1 (10)) for the antenna ports, as shown in Figure 5 below.

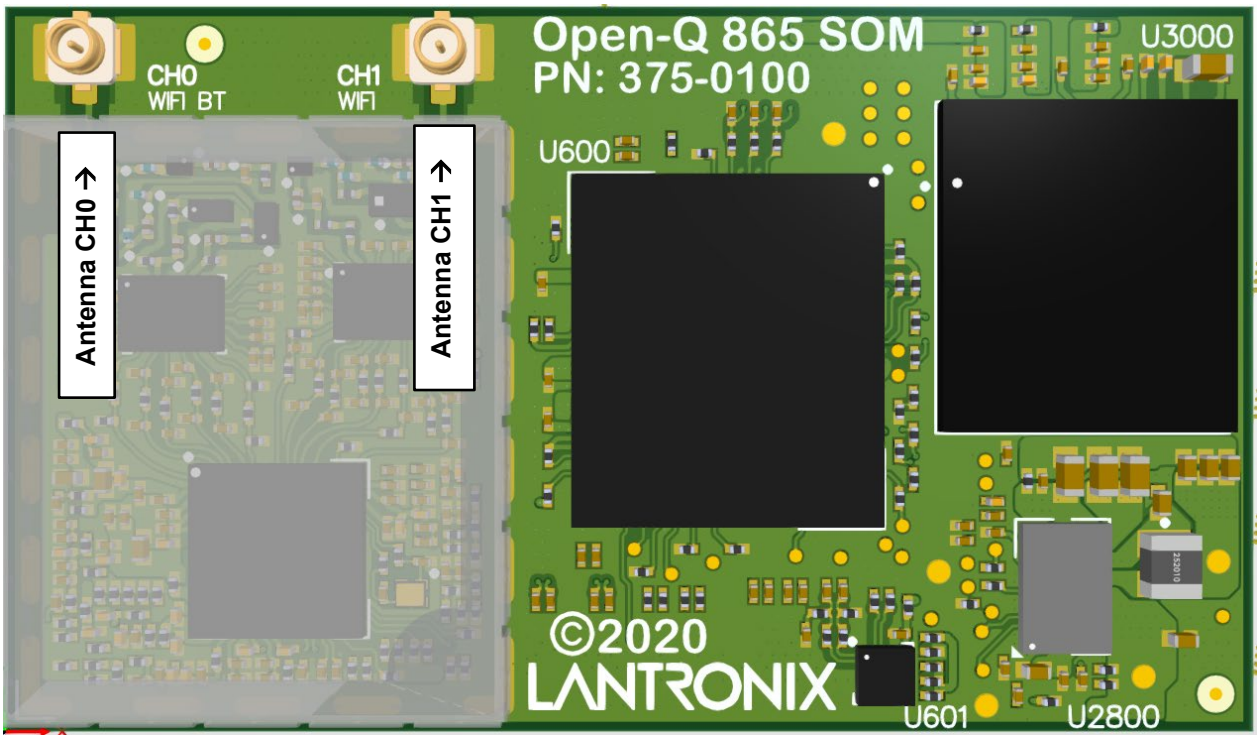

Figure 5. Antenna Connection Locations on SOM

Table 5. RF Signals via U.FL Coaxial Receptacles

Antenna	Description	Notes
Antenna CH0	RF chain 0 interface to Qualcomm QCA6391 chipset for Wi-Fi/BT	Antenna port for Wi-Fi and Bluetooth
Antenna CH1	RF chain 1 interface to Qualcomm QCA6391 chipset for Wi-Fi	Second antenna port for Wi-Fi 2x2 MIMO

5 Electrical Specifications

The input power to the SOM is provided by a power supply (battery or wall adapter) and a USB source, for battery charging purposes. All input power sources enter the PM8150B power management IC on the SOM, which then distributes power (along with the PM8150L, PM8250 and PM8009 PMICs) to other circuits on the SOM and connected carrier board via LDO and switching power supply outputs.

5.1 Absolute Maximum Ratings

Table 6 shows the absolute maximum ratings in which the SOM input power sources can be exposed to without experiencing functional failure.

Table 6. Absolute Maximum Input Power Ratings

Parameter	Min	Max	Units
Battery or DC power input (SOM_SYS_PWR)	-0.3	6	V
USB VBUS battery charger input voltage source (USB_VBUS)	-0.3	28	V

5.2 Operating Conditions

Table 7 shows the recommended operating conditions for the SOM to meet all performance specifications (provided the absolute maximum ratings have never been exceeded).

Table 7. Operating Input Power Ratings

Parameter	Min	Typ	Max	Units
Battery or DC power input (SOM_SYS_PWR)	3.45 [1]	3.8	4.8	V
USB VBUS battery charger input voltage source (USB_VBUS)	3.6	5	12	V
VCOIN Input	2.0	3.0	3.25	V

5.3 Operating Temperature

The SOM operating temperature ratings listed in Table 8 are based only on the operating temperature grade of the SOM components. Users should consider the specific environmental conditions in which the final product is used in.

Table 8. Input Power Ratings for Operational Use

Parameter	Min	Typ	Max	Units
Overall SOM (case temperature)	-25	+25	+85	°C

[1] The SOM may be configured to operate at lower input voltage levels but changes to bootloader or proprietary code are needed and this will require support from Lantronix. Lantronix's solutions and software engineering services can provide advice and support for specialty low voltage requirements. Please contact Lantronix sales: http://www.lantronix.com/about-us/contact/

5.4 Power Consumption

Table 9 below shows the SOM power consumption numbers under common operational modes when data is available.

Table 9. Power Consumption Ratings

Operational Modes	Description	Average	Peak
Boot	Power consumption during boot process	N/A	TBD
Suspend (Wi-Fi Off)	SOM placed in standby (Wi-Fi Off, Display Off)	TBD	N/A
Suspend (Wi-Fi On)	SOM placed in standby (Wi-Fi On, Display Off)	TBD	N/A
Idle (Display On)	SOM is idle (Wi-Fi Off, Display On)	TBD	TBD
Idle (Display Off)	SOM is idle (Wi-Fi Off, Display Off)	TBD	TBD
Video Record (1080P)	SOM recording 1080P video (Wi-Fi Off, Display On)	TBD	TBD
Video Record (4K UHD)	SOM recording 4K UHD video (Wi-Fi Off, Display On)	TBD	TBD
Video Playback (1080P)	SOM playing back 1080p video (Wi-Fi Off, Display On)	TBD	TBD
Video Playback (4K UHD)	SOM playing back 4K UHD video (Wi-Fi Off, Display On)	TBD	TBD
Audio Playback	SOM playing back MP3 audio file (Wi-Fi Off, Display Off)	TBD	TBD
Wi-Fi Download	SOM downloading data via Wi-Fi (Display Off)	TBD	TBD
Wi-Fi Upload	SOM uploading data via Wi-Fi (Display Off)	TBD	TBD
Full Load (All Cores)	SOM running all CPU cores (Wi-Fi Off, Display Off)	TBD	TBD
Single Core	SOM running single core (Wi-Fi Off, Display Off)	TBD	TBD
Bluetooth	SOM playing music over Bluetooth (Wi-Fi Off, Display Off)	TBD	TBD

5.5 ESD Ratings

The SOM is not designed with additional ESD protection other than what is included in the integrated circuits. It is recommended to take proper precautions in a static free environment when handling the SOM.

6 Mechanical Specifications

The sections below present some mechanical details of the Open-Q 8250CS SOM. For access to the 3D design files, please see https://tech.intrinsyc.com **Error! Hyperlink reference not valid.**(development kit registration required).

6.1 SOM Mechanical Outline

The outer dimensions of the SOM are 50.0 x 29.0mm, as shown in Figure 6 below. PCB thickness is nominally 0.99mm.

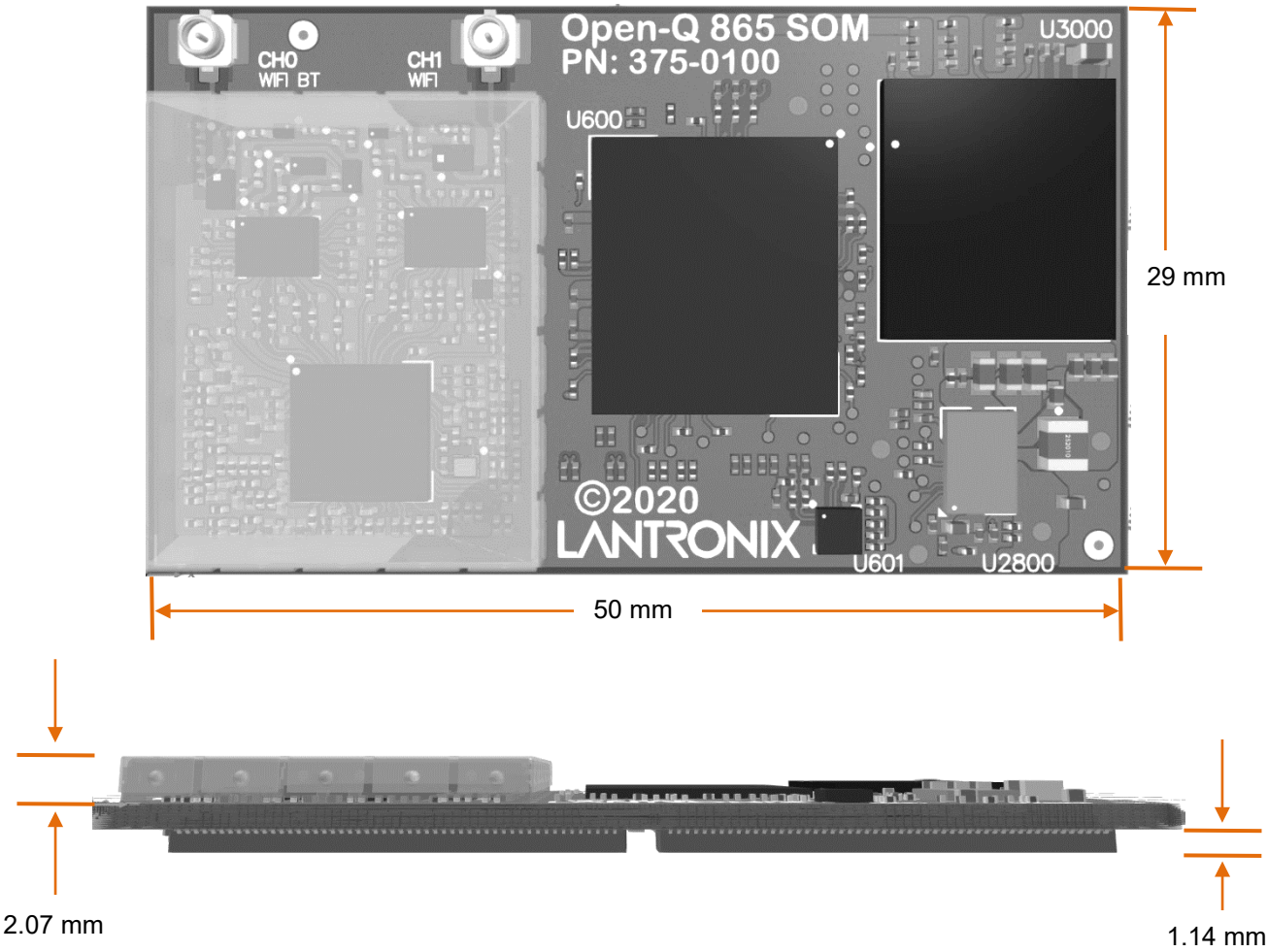

Figure 6. SOM Mechanical Outline (mm)

6.2 Top and Bottom Height Restrictions

The tallest component on the top-side of the SOM is the Wi-Fi shield at 2.07 mm (nominal, see Figure 6 above). Please note that when the mating coax cables are connected, the top side height may be higher.

The tallest component on the bottom-side of the SOM is the board-to-board connectors at 1.14mm (nominal, see Figure 6 above).

6.3 Landing Pattern

The footprint information in this section can be used as a guide when designing a landing area for the SOM.

Dimensions show the relative position of each connector on the SOM; referenced to the center of the connector body.

***Note**: This information is given for reference. Please see the SOM Carrier Board Design Guide for more detail (Reference Document R-2).*

*The perspective of this figure is looking at the bottom side of the SOM.

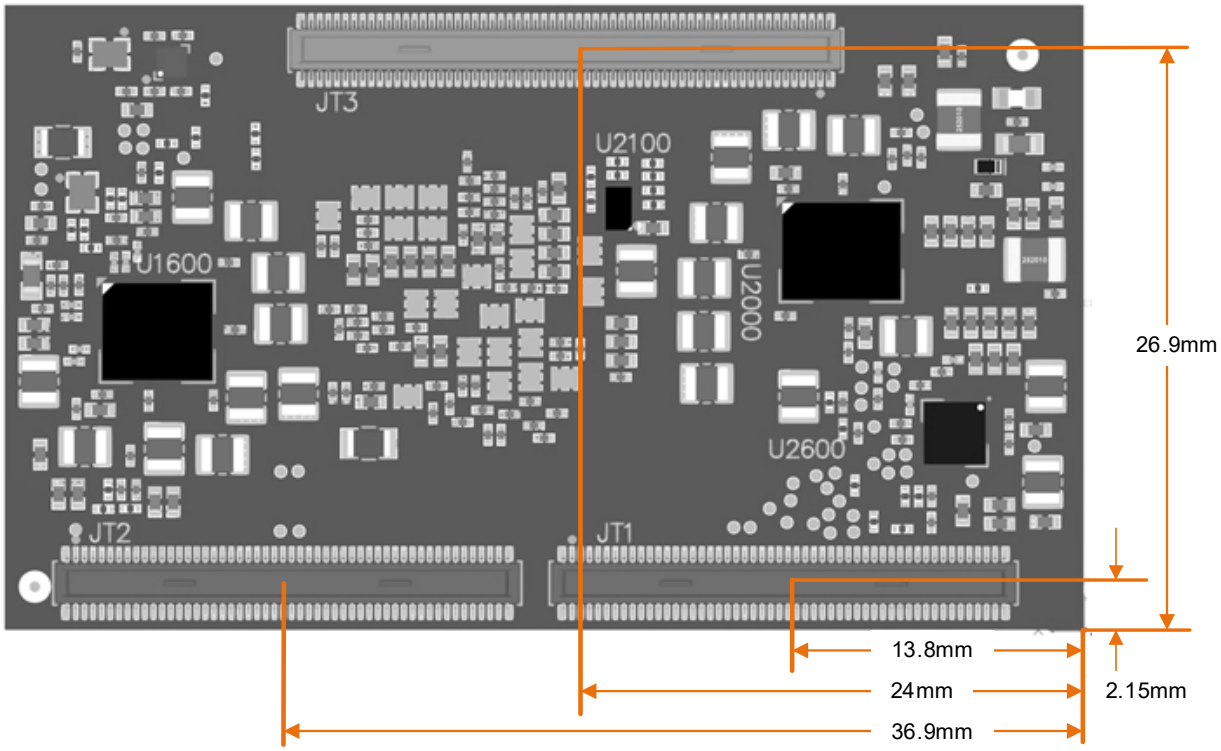

Figure 7. SOM Land-Pattern Dimensions (mm)

The mating connectors, Hirose DF40C-100DS-0.4V and Hirose DF40C-120DS-0.4V, are available in different heights, to achieve stack heights of 1.5mm or 3.0mm.

6.4 Thermal Characteristics

The QCS8250 CPU has built-in thermal protections which will reduce processor frequency as the die temperature approaches set operating limits. These limits protect the processor from damage that could be caused by elevated die temperature. Additional product-level thermal management will remove heat from the SOM and its components, allowing the processor to run at higher frequencies for longer time periods before approaching the built-in die temperature limits. This enables the average processor speed to remain higher through processor-intensive applications. Effectively removing heat from the Open-Q 8250CS SOM is required to optimize system performance and efficiency and to ensure that the QCS8250 CPU processor can perform as desired.

For more information on thermal mitigation, see the SOM Carrier Board Design Guide (Reference Document R-2).

6.5 Weight

The SOM weighs approximately 6 grams.

7 Product Marking, Ordering, and Shipping Info

7.1 Product Marking

The SOM part number and product marking can be identified on the white label on the top of the module. Figure 8 shows a label example which includes the SOM name and QR code.

Figure 8. Open-Q 8250CS SOM Label (top of PCB)

Table 10 describes the SOM label in additional detail.

Table 10. Open-Q 8250CS SOM Label Marking Details

Line	Marking	Description/ Notes
1	Open-Q 8250CS SOM	LANTRONIX Product Name

2	QR code *	Embeds serial number and Wi-Fi MAC address. The serial number format** is **VVV-WXXX-YYYYYY-ZZZZZ**:
		• **VVV** = Product number
		• **W** = SKU variant. For the Open-Q 8250CS:
		  ○ B: QC-SOM-8250CS-A
		• **XXX** = Part number revision
		  ○ Example: A11. Alpha (A) represents a software change and numeric (11) represents a hardware change.
		• **YYYYYY** = Date of manufacture (mm/dd/yy)
		• **ZZZZZ** = Unique serial number for PCB
		The MAC address format is 0123456789AB
		12 hexadecimal digit MAC address

* QR code reader mobile app (e.g. Neo Reader) can be used to read embedded serial number and the MAC address. ** Older serial number format (differences shown in bold) is: **VVV-WWXX-YYYYYY-ZZZZZ** • **VVV** = Product number • **WW** = PCB revision number • **XX** = BOM revision number • **YYYYYY** = Date of manufacture (mm/dd/yy) **ZZZZZ** = Unique serial number for PCB		

7.2 Product Ordering Information

The Open-Q 8250CS SOM can be ordered for evaluation and prototype use from Lantronix. For volume production orders or for custom requirements please contact sales at http://www.lantronix.com/about-us/contact.

Table 11. Orderable Part Numbers

Description	SKU
Open-Q 8250CS SOM std memory (128GB UFS + 8GB DDR)	QC-SOM-8250CS-A

7.3 Packaging and Shipping Information

The Open-Q 8250CS SOM is packaged individually in small anti-static bags and bubble-wrap bags for protection during shipping – see Figure 9 below. They are then put into different sized boxes depending upon the quantity of the order. Small quantities are shipped in standard courier boxes with bubble-wrap protection and large quantity orders are packaged in a carton with dividers, as shown in Figure 10 below.

Figure 9. Individual SOM Packaging

Figure 10. Packaging for Large Quantity Shipments

8 Handling Precautions

8.1 ESD Precautions

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

The Open-Q 8250CS SOM is designed as a component meant to be integrated into a final product and therefore has no additional ESD protection built-in. It should be handled only in a static-safe environment to prevent damage.

8.2 SOM / Carrier Board Mating Precautions

WARNING:

In order to prevent damage, caution must be taken when inserting or removing the SOM from the carrier board. When inserting the SOM, ensure that the three board to board connectors are aligned between the SOM and carrier board. The SOM should be inserted with only straight up and down force along both long edges of the SOM where the board-to-board connectors are located. Any sideways force on the connectors must be avoided. Force should be applied until the SOM is fully seated on the carrier board connectors. See Figure 11 to view the top-down pressure locations.

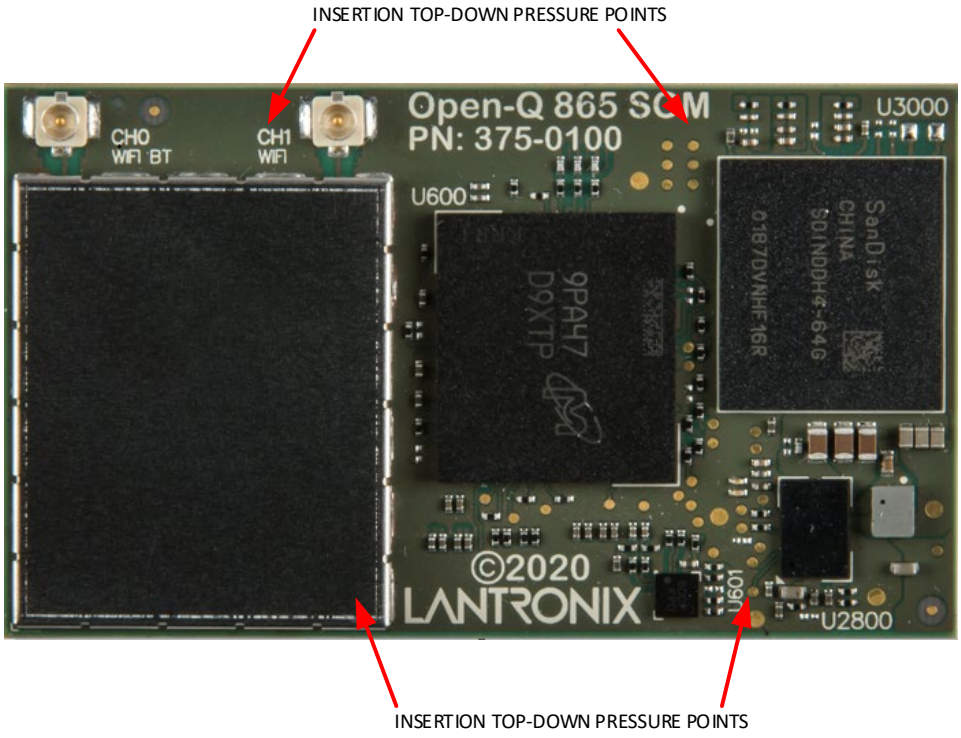

Figure 11. SOM Insertion Top-Down Pressure Locations

When removing the SOM from the carrier board, a plastic prying tool (see ifixit.com for examples) is recommended to gradually raise the SOM on alternating short sides until it is free of the carrier board. See Figure 12 to view the recommended prying tool removal locations.

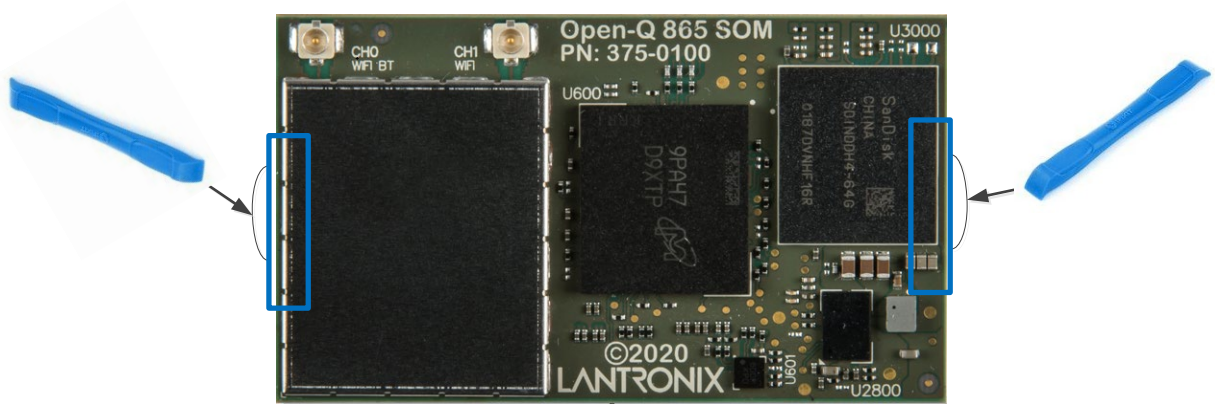

Figure 12. SOM Plastic Prying Tool Removal Locations

As mentioned above, the SOM should be raised gradually on alternating short sides. Do not attempt to raise one side entirely. Also, raising the SOM from the long side of board edge (red marked areas in the figure above) MUST be avoided. See Figure 13 below for these warnings.

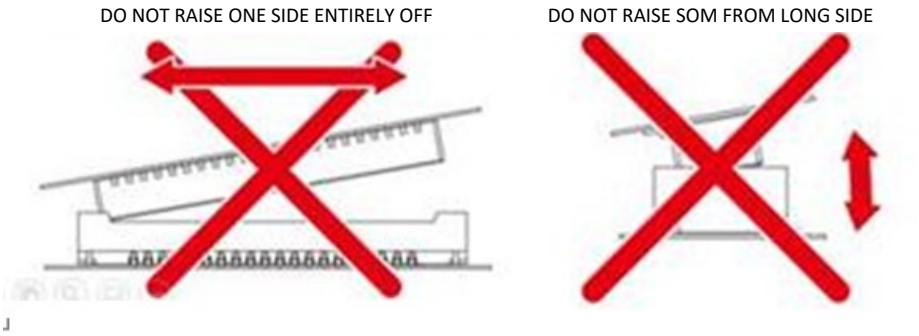

Figure 13. SOM Extraction Warnings

Also note that the Hirose DF40 board-to-board connector series are rated for a maximum of 30 mating / un-mating cycles. Therefore, the number of SOM insertions and removals must be limited to ensure connector reliability.

8.3 Storage Conditions

The SOM must be stored in an antistatic bag.

Table 12. Recommended Storage Conditions

Temperature/Humidity	Range
Temperature	-40 -> +85 °C
Humidity (non-condensing, relative)	5% -> 85 %

9 Certification

9.1 Radio Certification

The Lantronix Open-Q 8250CS SOM is certified with FCC and Industry Canada as a modular radio transmitter for WLAN and Bluetooth. The FCC ID and Industry Canada ID numbers are listed below.

- FCC ID: R68OQ865S
- ISED (Canada): 3867A-OQ865S

The Lantronix Open-Q 8250CS SOM has also obtained the CE EU Declaration of Conformity certificate.

These certifications apply so long as the antenna structures and transmit powers used are equivalent to those used for the original certification. Changes to firmware, drivers, or board configuration files may have an impact to transmit power. For this reason, it is recommended to refer to the SOM certification documents (see Reference Document R-4) for information regarding the test configurations used for certification. Deviating from the documented configuration may trigger the need for re-certification.

9.2 ROHS/REACH Compliance

The Lantronix Open-Q 8250CS SOM complies with the ROHS/REACH standard. The certificate is available at www.lantronix.com.