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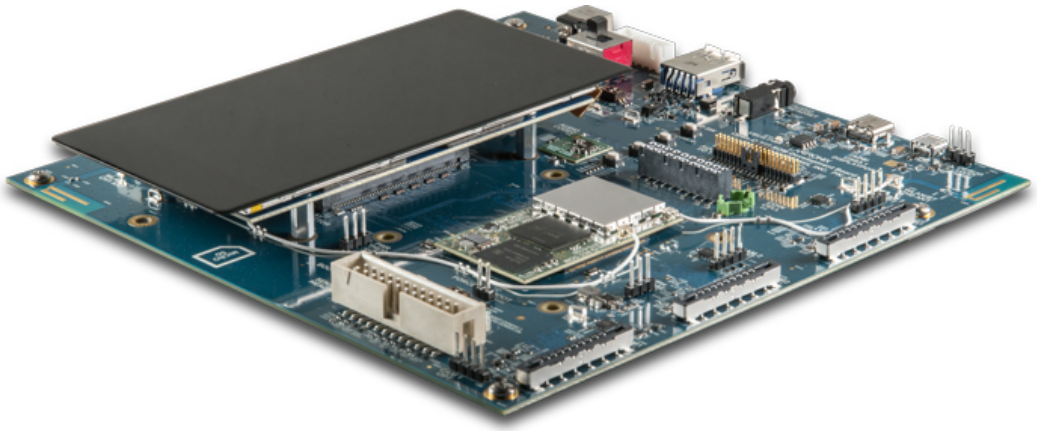

Open-Q™ 865XR SOM Development Kit User Guide

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Revision History

Date	Rev.	Comments
August 2020	A	Preliminary Initial Lantronix document
October 2020	B	General document updates and new section 3.6.1.

For the latest revision of this product document, please go to: http://tech.intrinsyc.com.

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1 Introduction

1.1 Purpose

The purpose of this user guide is to provide instructions and technical information on the Open-Q 865XR SOM Development Kit.

You can find information on this and other Lantronix development kits on the Lantronix web site: http://www.lantronix.com/products

1.2 Scope

This document will cover the following items on the Open-Q 865XR SOM Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- SOM
- Carrier Board
- Available peripherals

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Lantronix Open-Q 865XR SOM Development Kit.

2 Documents

This section lists the supplementary documents for the Open-Q 865XR SOM Development Kit.

2.1 Applicable Documents

REFERENCE	TITLE
A-1	Intrinsyc License and Purchase Terms and Conditions for the Open-Q 865XR SOM

2.2 Reference Documents

The below listed documents are available on the Technical Portal: https://tech.intrinsyc.com (dev kit registration required)

REFERENCE	TITLE
R-1	Open-Q 865XR SOM HW Datasheet
R-2	Open-Q 865XR SOM Carrier Board Design Guide
R-3	Open-Q 865XR SOM Schematics (SOM and Carrier)
R-4	Open-Q 865XR SOM Development Kit – Display Adapter Design Guide
R-5	Open-Q 865XR SOM Development Kit – Camera Adapter Design Guide
R-6	Open-Q 865XR SOM Development Kit – Battery Charging Tech Note

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission

FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
QUP	Qualcomm Universal Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SOM	System on Module
SPMI	System Power Management Interface (Qualcomm PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

3 Open-Q 865XR SOM Development Kit

3.1 Introduction

The Open-Q 865XR provides a quick reference and evaluation platform for the Qualcomm SXR2130P Platform. The development kit is suited for Android application developers, OEMs, consumer manufacturers, hardware component vendors, camera vendors, and product designers to evaluate, optimize, test and deploy applications that can utilize the Qualcomm SXR2130P Platform technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at

http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 865XR SOM Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap.

3.4 Development Kit Contents

The Open-Q 865XR SOM Development Kit comes with Android software pre-programmed and includes the following:

- Open-Q 865XR SOM with the Qualcomm SXR2130P processor
- Mini-ITX form-factor carrier board
- AC power adapter

3.4.1 Important Locations

The diagram below shows the locations of key components, interfaces, and controls.

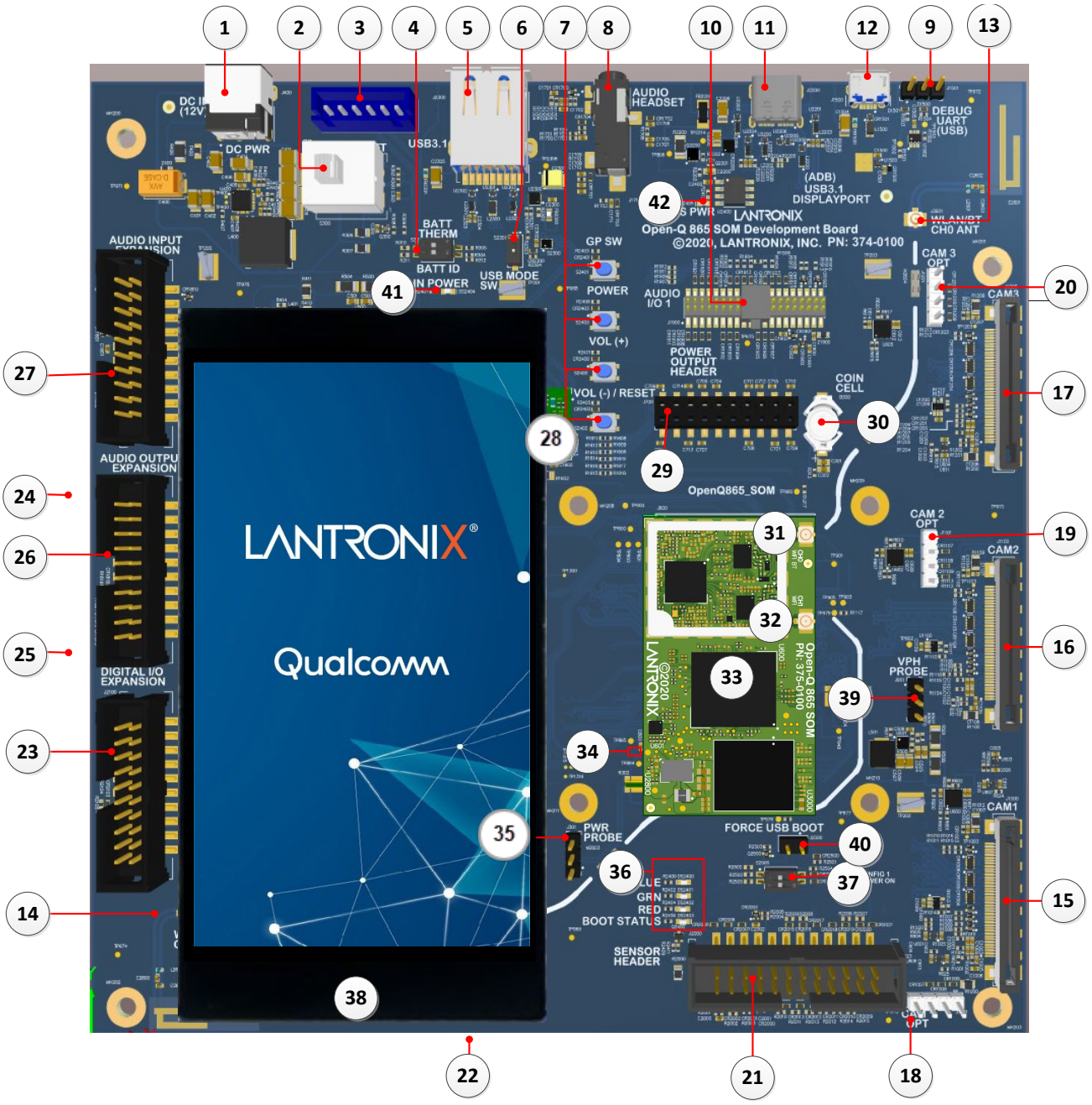

Figure 1. Assembled Open-Q 865XR SOM Development Kit

Table 1. List of Development Kit Features itemized in the figure above

Position	Feature Description	Reference Designator
1	DC Power Supply Jack	J400
2	Power Source Selector	S300
3	Battery Input Header	J300
4	Battery Configuration DIP Switch	S301
5	USB 3.1 Type A Connector	J2300
6	M.2 PCIe USB Enable DIP Switch	S2301
7	Buttons: General Purpose / Power / Volume Up / Volume Down	S2401 / S2403 / S2400 / S2402
8	Audio Headset Jack	J1700
9	Debug UART Header	J1501
10	Audio I/O Header	J1900
11	USB 3.1 Type-C connector for ADB	J2200
12	USB Serial Debug Console	J1500
13	WLAN/BT Channel 0 External Antenna Connector	J2601
14	WLAN Channel 1 External Antenna Connector	J2600
15	Camera 1 Connector	J1000
16	Camera 2 Connector	J1100
17	Camera 3 Connector	J1200
18	Camera 1 Option Header	J1001
19	Camera 2 Option Header	J1101
20	Camera 3 Option Header	J1201
21	Sensors Expansion Header	J2000
22	Micro SD card socket (on bottom side of Carrier Board)	J1400
23	Digital IO Expansion Header	J2100

Position	Feature Description	Reference Designator
24	M.2 PCIe Card Connector (on bottom side of Carrier Board)	J2700
25	SIM Card Socket for M.2 PCIe (on bottom side of Carrier Board)	J2701
26	Audio Outputs Expansion	J1801
27	Audio Inputs Expansion	J1800
28	Audio Codec Module (on top side of Carrier Board underneath Display Adapter)	U1600
29	Power Header	J700
30	Coin Cell Holder	B300
31	Open-Q 865XR SOM, WLAN/BT CH0 Antenna Connector	J3700 (on SOM)
32	Open-Q 865XR SOM, WLAN CH1 Antenna Connector	J3800 (on SOM)
33	Open-Q 865XR SOM	
34	On-Board Quiet Thermistor	RT800
35	SOM Current Sense Probe Header(SOM_SYS_PWR)	J301
36	LEDs: (BOOT State / Blue / Green / Red)	DS2403 / DS2400 / DS2401 / DS2402
37	System Configuration DIP Switch	S2500
38	Open-Q LCD Panel	
39	SOM Current Sense Probe Header(VPH_PWR)	J901
40	Force USB Boot Header	J2500
41	Main Power LED	DS2407
42	VBUS LED	DS2405

3.4.2 Block Diagram

The block diagram below shows the connectivity and major components of the Open-Q 865XR SOM Development Kit.

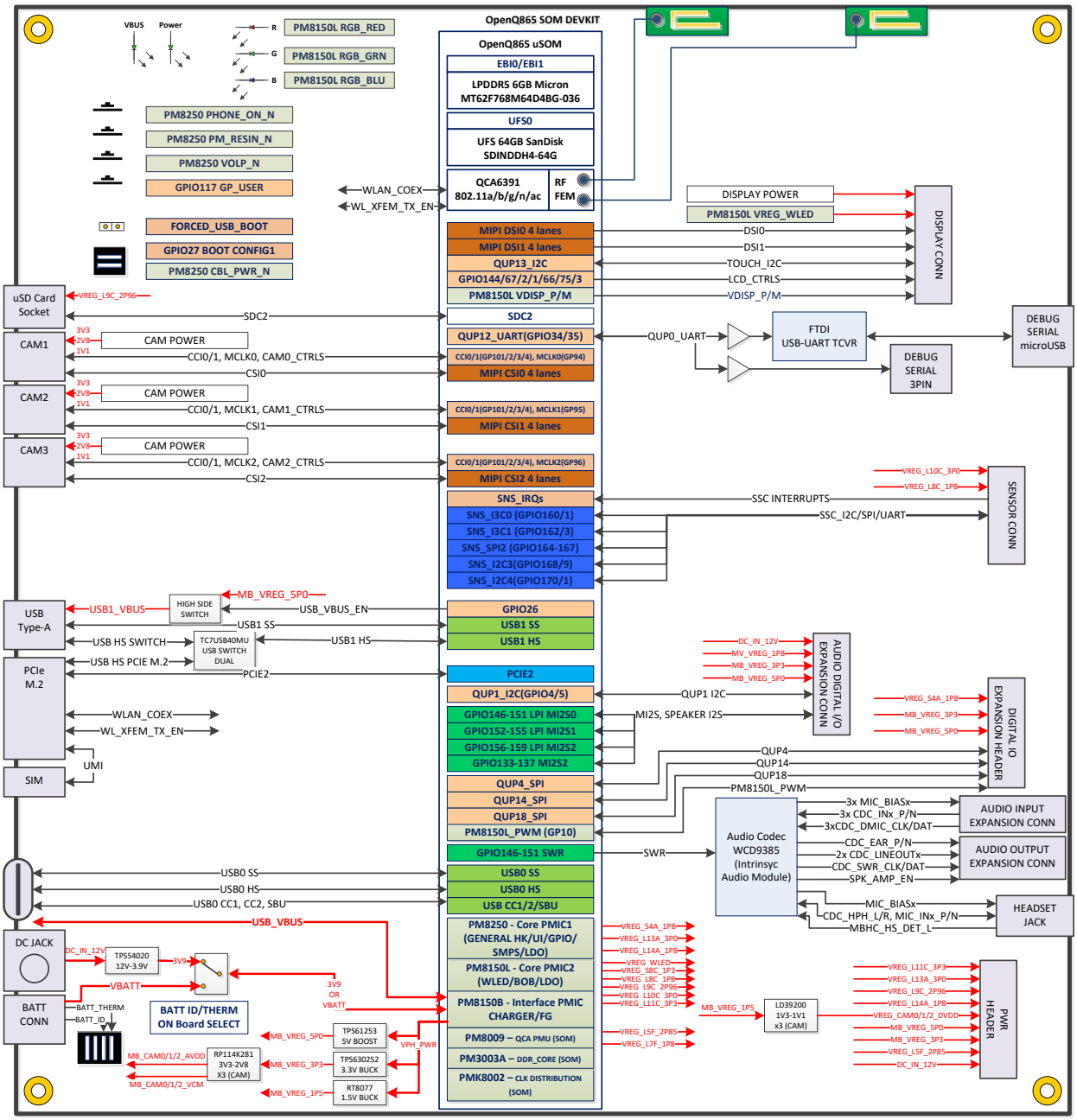

Figure 2. Open-Q 865XR SOM Dev Kit Block Diagram

3.4.3 Optional Accessories

Optional accessories are available for the Open-Q 865XR SOM Development Kit, like LCD Panel, Camera adapter, and sensor board. Please visit the product store for availability of these

accessories: https://shop.intrinsyc.com/collections/accessories, or contact sales@lantronix.com.

3.5 Getting Started

This section explains how to setup the Open-Q 865XR SOM Development Kit and start using it.

3.5.1 Registration

To register the development kit and gain access to the Intrinsyc Technical Document Portal, please visit: http://tech.intrinsyc.com/account/register.

To proceed with registration, the development kit serial number is required. These serial numbers can be found on the labels that are present on the SOM and carrier boards. The labels contain the following information:

- SOM: Serial Number, WIFI MAC address
- Carrier: Serial Number

Note: Please retain the SOM and carrier board serial numbers for warranty purposes.

Refer to http://tech.intrinsyc.com/account/serialnumber for more details about locating the development kit serial number.

3.5.2 Configuration Switch Settings

The default configuration for the system configuration DIP switch S2500 is for all switches to be open or OFF and Header J2500 is open. For details about other configurations, see section 3.7.2.

3.5.3 Powering Up the Development Kit

The development kit can be powered up by either using a DC power supply or by connecting a battery on connector J300. Select the desired power source using the switch S300 on the carrier board. The green LED DS2404 marked “POWER” on the board is the power LED and should glow once the development kit is powered. To see the debug logs, connect a serial debug cable to the J1500 connector.

To power-up the board, perform the following exact steps below detailed below:

1. At a static-safe workstation, remove the development kit board carefully from the anti-static bag.
2. Connect the Power Adapter to the 12V DC Jack J400 and then press and hold the power button until you see the company logo appears on the on-board display (~3 seconds).
3. Navigate using the touchscreen on the on-board display.

3.6 Open-Q 865XR SOM

The Open-Q 865XR SOM contains the core 865 architecture. Measuring in at 50mm x 29mm, the SOM is where all the processing occurs. It is connected to the carrier board via two 100 pin and one 120 pin Hirose DF40 connectors which allows essential power rails and signals to be exposed for supporting other peripherals and interfaces on the platform.

For detailed information about the Open-Q 865XR SOM, see the datasheet noted as reference document R-1.

3.6.1 SOM / Carrier Board Connector Mating Precautions

WARNING:

In order to prevent damage, caution must be taken when inserting or removing the SOM from the carrier board. When inserting the SOM, ensure that the three board to board connectors are aligned between the SOM and carrier board. The SOM should be inserted with only straight up and down force along both long edges of the SOM where the board to board connectors are located. Any sideways force on the connectors must be avoided. Force should be applied until the SOM is fully seated on the carrier board connectors. See Figure 3 below.

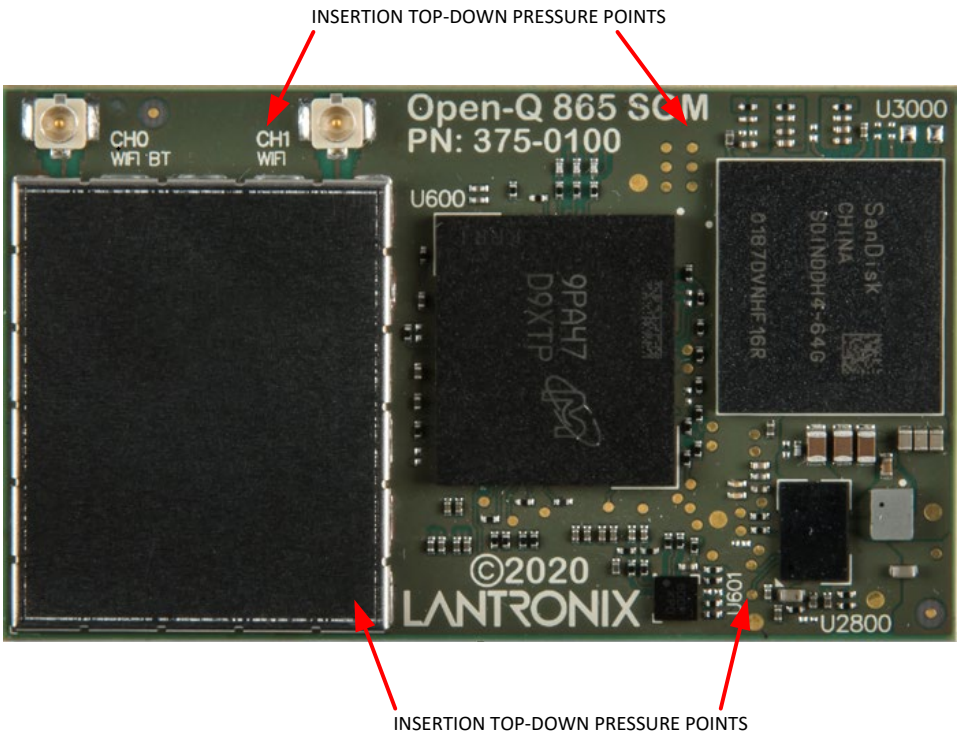

Figure 3. SOM Insertion Top-Down Pressure Locations

When removing the SOM from the carrier board, a plastic prying tool (see ifixit.com for examples) is recommended to gradually raise the SOM on alternating short sides until it is free of the carrier board. See Figure 4 below.

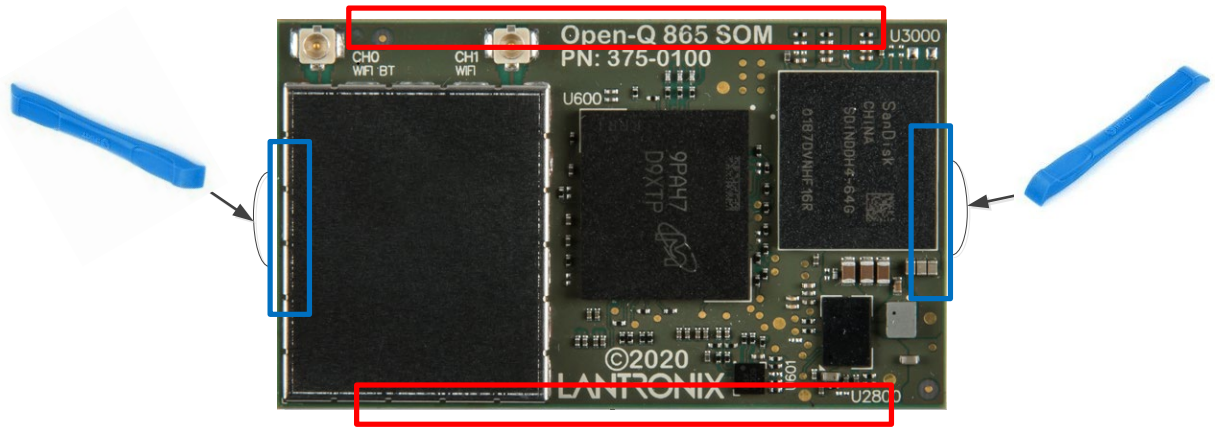

Figure 4. SOM Plastic Prying Tool Removal Locations

As mentioned above, the SOM should be raised gradually on alternating short sides. Do not attempt to raise one side entirely. Also, raising the SOM from the long side of board edge (red marked areas in the figure above) MUST be avoided. See Figure 5 below for these warnings.

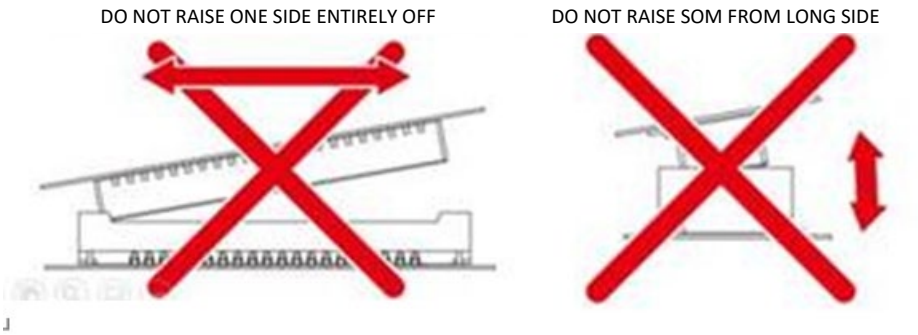

Figure 5. SOM Extraction Warnings

Also note that the Hirose DF40 board to board connector series are rated for a maximum of 30 mating / un-mating cycles. Therefore, the number of SOM insertions and removals must be limited to ensure connector reliability.

3.7 Open-Q 865XR SOM Carrier Board

The Open-Q 865XR SOM Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals. The table and sections below provide in depth information on the carrier board properties, user interfaces, connectors, and expansion headers found on the carrier board. This information is important for users wishing to connect other external hardware devices to the Open-Q 865XR SOM Development Kit. Users must ensure that before connecting any hardware device to the development kit, that it is compatible with the Open-Q 865XR hardware specifications. See Figure 1 for position on carrier board.

Table 2. Carrier Board Features

Item	Position	Description	Specification	Usage
Form Factor		Dimensions: 170mm x 170mm	Mini-ITX Form Factor	
SOM Interface	33	2 x 100-pin Hirose DF40 connectors 1 x 120-pin Hirose DF40 connector	SOM power and signal IO connection to carrier board.	The Open-Q 865XR SOM connects to the carrier board through this interface.
Power	1	AC / Barrel charger	12 V DC Power Supply	Power Supply
Power	3	Battery connector for single cell lithium battery		Input power option
Debug Serial via USB	12	Debug Serial UART console over USB for development	USB Micro B connector	Development Serial Connector for debug output via USB
Buttons	7	General Purpose SW button	SMD Button	Additional button for general purpose
	7	Power Button	SMD Button	Power Button for Suspend / Resume and Power off
Volume Keys	7	Volume + key	SMD Button	Volume +Key
	7	Volume – key	SMD Button	Volume – Key
Sensor Connector	21	24 pin Sensor Expansion Connector		Available via Lantronix optional accessories kit
Digital IO Expansion Header	23	Exposes general purpose IO for user development		
Audio Headset Jack	8	Audio Headset Jack		Audio Headset
Audio Inputs Expansion	27	Audio Inputs Header	3 Analog Differential Inputs, 3 PDM Input Interfaces with phantom power	Microphones
Audio Outputs Expansion	26	Audio Outputs Header	2 Line outputs, 1 earphone amplifier output, 1 Soundwire interface	Amplifiers
Audio I/O	10	Audio I/O headers	3 x I2S, 1x Analog Differential Input	Various audio I/O functions
UART header	9	3 pin header	1.8V UART debug header	UART debug
Micro SD (on bottom)	22	Micro SD card	4bit Micro SD card support	External Storage
USB Type C	11		USB 3.1 type C connector	For USB debugging and client / host mode

Item	Position	Description	Specification	Usage
USB Type A	5		Female Type A Connector	USB 3.1 Host interface
WLAN Antennas	13, 14	2 PCB Antennas		Coax connection to SOM WiFi module
Coin Cell Holder	30	Coin Cell battery holder provided	for PMIC RTC	
LEDs	36/41/42	Six LEDs	Three user driven LEDs	
LCD Display and Touch connector	38	100 pin for LCD signals	2x 4-lane MIPI DSI MIPI Alliance Specification for DPHY v1.2	For connecting display accessory
CSI Camera connectors	15, 16, 17	3x camera connectors	MIPI Alliance Specification for CSI-2 v1.3	For connecting camera accessories.
Camera option header	18,19,20	4 pin header	Camera option header	Not connector anywhere else on the CB and is expected to be connected via wires to other GPIO headers on the dev kit if desired to be used by the dev kit user.
Current Sense Header (VPH_PWR)	35	3 pin header	Sense lines connected across 0.005 Ohm resistor	To measure current consumption of SOM_VPH_PWR
Current Sense Header (SOM_SYS_PWR)	39	3 pin header	Sense lines connected across 0.005 Ohm resistor	To measure current consumption of SOM_SYS_PWR
M.2 PCI Express Connector (on bottom)	24	M.2 PCI Express for external peripheral connectivity	M.2 PCI Express B-Key interface.	For external M.2 PCIe card
WWAN SIM Card (on bottom)	25	WWAN SIM card connector (optional)		For WWAN M.2 PCI express cards

3.7.1 SOM Board to Board Connectors (33)

The Open-Q 865XR SOM connects to the carrier board via two 100 pin and one 120 pin Hirose DF40 connectors which allows essential power rails and signals to be exposed for supporting other peripherals and interfaces on the platform. For the list of signals exposed by the SOM, see the SOM datasheet (Ref. R-1).

3.7.2 Boot Configuration DIP Switch S2500 (37)

There is a DIP switch S2500 and one 2pins header on the top side of the Open-Q 865XR SOM carrier board. The 2-bit switch allows the user to control the system configuration and boot options. The 2pins header is for Force USB Boot mode select. The image below shows the DIP switch and header assignments.

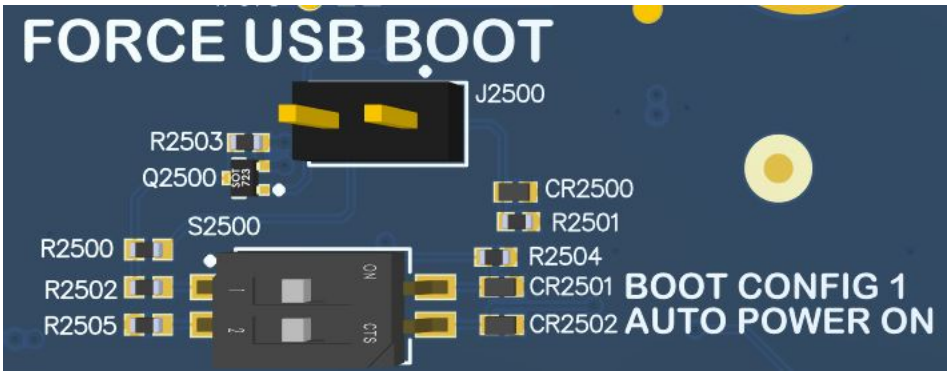

Figure 6. DIP switch assignments

See the table below for a description of the DIP switch and header connections.

Table 3. Boot Configuration DIP Switch & Header Settings

Function	DIP Switch/Header	Description	Notes
BOOT_CONFIG[1]	S2600-1	CPU boot configuration bit 1. Connected to CPU GPIO27	For default boot configuration, leave open / OFF. Other boot configurations not supported.
CBL_PWR_N	S2500-2	Controls the auto boot of the SOM when power is applied.	Default configuration is open / OFF. To enable auto boot of the SOM when power is applied, set switch closed / ON.
FORCED_USB_BOOT	J2500	For factory mode programming. Connected to CPU GPIO132.	For Lantronix use only. Leave open.

3.7.3 Input Power Selection

The development kit can be powered using either external DC power supply or by using a battery. The input power source selection is performed by using the connectors and selection switches shown in the figure and subsections below.

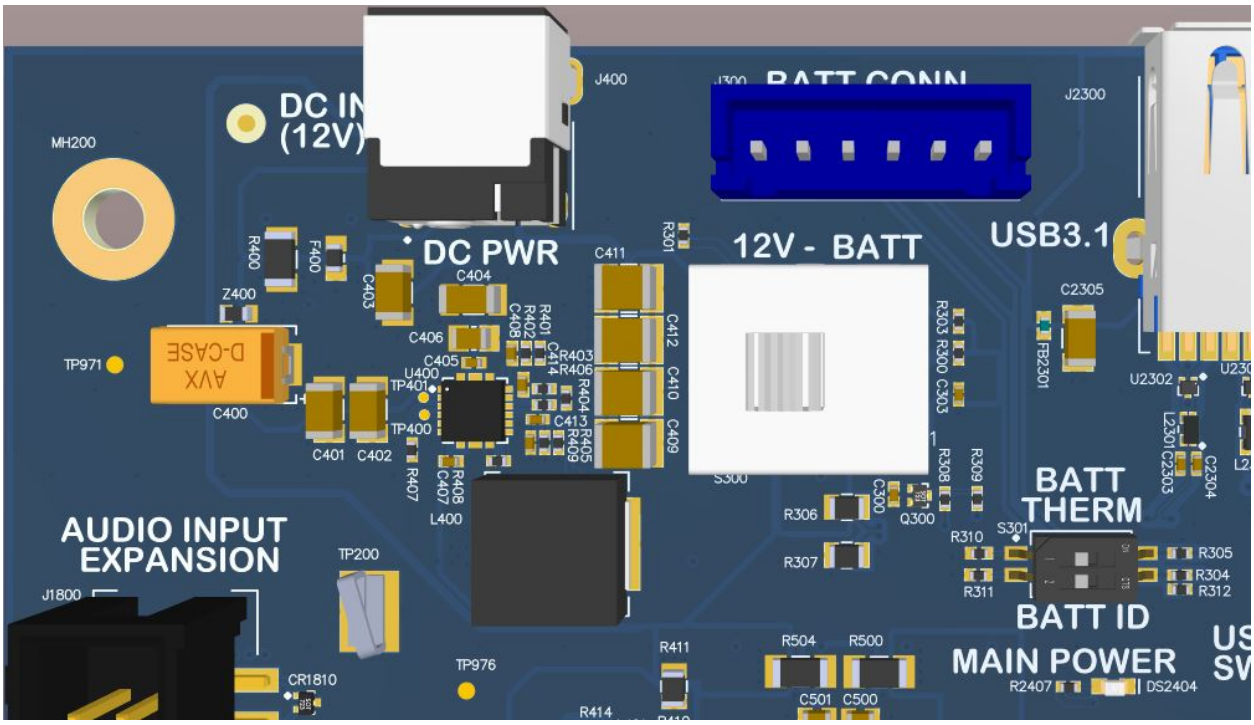

Figure 7. Input Power Selection Locations

3.7.3.1 Input Power Selection Switch S300 (2)

The S300 switch shown in the figure above is used to select the power source. To select the external DC power supply as the power source, slide the switch towards the '12V' position. To power up the kit using the battery, slide the switch towards the 'BATT' position. The default position is '12V'.

3.7.3.2 Battery ID and Thermistor Configuration DIP Switch S301 (4)

The 2-position DIP switch S301 shown in the figure above configures the battery ID and thermistor settings. The table below describes the settings for the battery ID / thermistor DIP switch.

Table 4. Battery ID / Thermistor Configuration DIP Switch Settings

Function	DIP Switch	Description	Notes
BATTERY THERMISTOR	S301-1	Selects whether or not a 100K ohm thermistor is attached to the battery connector J300.	For DC powered dev kit, set switch to closed / ON (default). This enables the use of the 'fake' 100K thermistor on the carrier board. For battery powered dev kit, set switch to open / OFF if thermistor is included on the battery pack. Otherwise keep switch closed / ON.
BATTERY ID	S301-2	Informs the 865XR SOM whether a valid battery is connected. The setting is used as input to enable or disable battery charging.	For DC power dev kit, set switch to closed / ON (default) to disable battery charging. For battery power dev kit, set switch to open / OFF to enable battery charging. For details on how to use this signal with a custom battery pack, see document R-6.

3.7.3.3 DC Power Input Jack J400 (1)

For a DC powered Open-Q 865XR SOM Development Kit, the DC power input jack J400 (see location in figure above) is used to connect to the include +12V DC power supply. The 865XR carrier board includes circuitry to convert the +12V input into different voltage rails that are needed by 865XR SOM and carrier board peripherals.

3.7.3.4 Battery Connector J300 (3)

For a battery powered Open-Q 865XR SOM Development Kit, the battery connector J300 (see location in figure above) is used for connection to the battery. The table below describes the pinout of the battery

connector. For more information on powering the development kit from a battery, including selecting a battery pack, see reference document R-6.

Table 5. Battery Connector J300 Pinout

Pin No	Signal	Description
1	GND	System ground, Battery Negative Wire
2	GND	System ground, Battery Negative Wire
3	BATT_THERM_CONN	100K Thermistor
4	BATT_ID_CONN	ID Resistor (optional)
5	VBATT_CONN	Battery Positive Wire
6	VBATT_CONN	Battery Positive Wire

3.7.4 Current Sense Header J301 (35) and J901 (39)

The SOM Current Sense header, J301, can be used to monitor the SOM + CB VPH_PWR current consumption on the main SOM_SYS_PWR power rail. The VPH Current Sense header, J901, can be used to monitor the CB VPH_PWR current consumption on the VPH_PWR power rail. The SOM power consumption can be calculated by: ((SOM + CB VPH_PWR) - (CB VPH_PWR)) power consumption. A close up of the J301(PWR PROBE) and J901(VPH PROBE) locations are shown below.

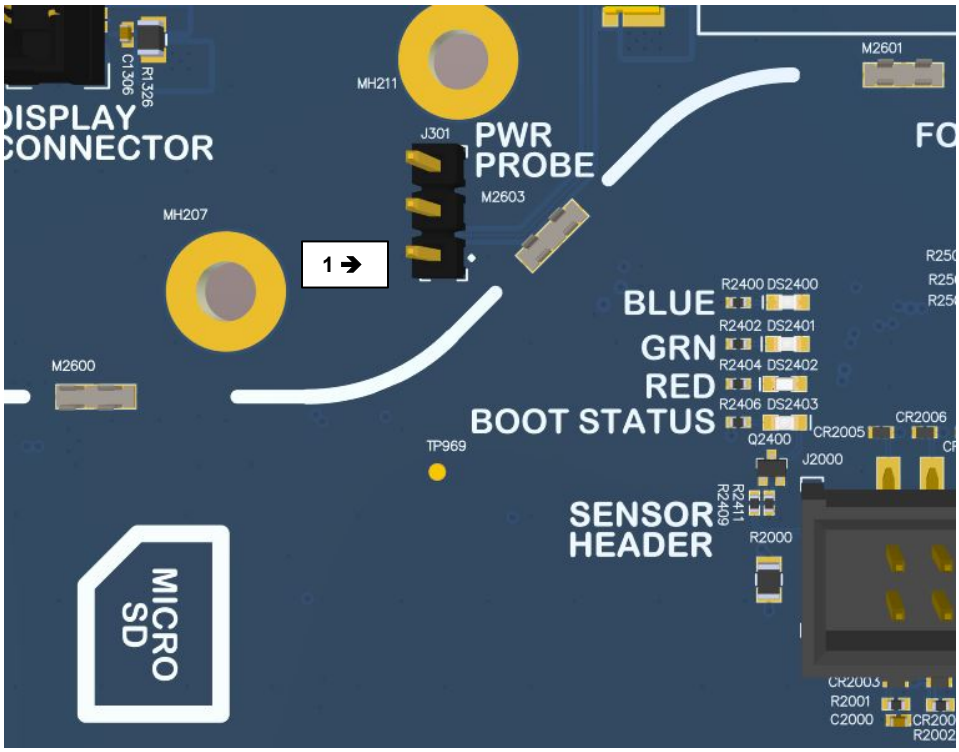

Figure 8. SOM Current Sense Header J301 (5)

The table below summarizes the pin outs of header J301

Table 6. Power Header J301 Pinout

Pin No	Signal	Description
1	SOM_PWR_SENSE_P	SOM power positive current sense line
2	SOM_PWR_SENSE_N	SOM power negative current sense line
3	GND	System Ground

To obtain power consumption measurements, the header is connected to a data acquisition unit (Keithley 2701 or similar) and the voltages on the SOM_PWR_SENSE_P/N pins are captured a few times a second over the test period (typically 30 minutes). The SOM power consumption is then calculated as (where Rsense = 5 milliohms):

$$P(som + vph\_pwr) = Vsom_{pwr_{sense_N}} * \frac{(Vsom_{pwr_{sense_P}} - Vsom_{pwr_{sense_N}})}{Rsense}$$

Use averaging to reduce noise.

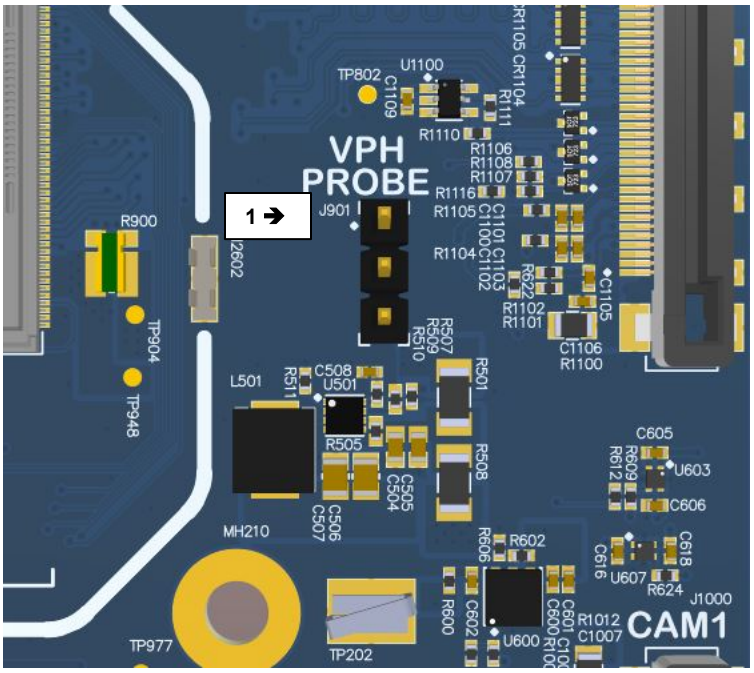

Figure 9. VPH Current Sense Header J901 (39)

The table below summarizes the pin outs of header J901

To obtain power consumption measurements, the header is connected to a data acquisition unit (Keithley 2701 or similar) and the voltages on the VPH_PWR_SENSE_P/N pins are captured a few times a second over the test period (typically 30 minutes). The SOM power consumption is then calculated as (where Rsense = 5 milliohms):

$$Pvph\_pwr = Vvph_{pwr_{sense_N}} * \frac{(Vvph_{pwr_{sense_P}} - Vvph_{pwr_{sense_N}})}{Rsense}$$

Use averaging to reduce noise.

Table 7. Power Header J901 Pinout

Pin No	Signal	Description
1	VPH_PWR_SENSE_P	VPH power positive current sense line
2	VPH_PWR_SENSE_N	VPH power negative current sense line
3	GND	System Ground

The SOM power consumption can be calculated by:

$$Psom = P(som + vph\_pwr) - Pvph\_pwr$$

3.7.5 Coin Cell Battery Holder B300 (30)

The coin cell holder allows the user to use a coin cell for supplying power to the SOM VCOIN power input. It is recommended that the Panasonic ML621 series rechargeable coin cell be used (not supplied with the development kit). See item 30 in Figure 1 for the coin cell battery holder location on the 865XR carrier board.

3.7.6 Power Header J700 (29)

The Power Header J700 provides access to various carrier board voltage rails. The pinout of the connector is listed in table below. See item 29 in Figure 1 for the power header location on the 865XR carrier board.

Table 8. Power Header J700 (29)

Pin No	Signal	Description	Pin No	Signal	Description
1	MB_ELDO_CAM0_DVDD_1P1	+1.1V Carrier Board LDO for Camera 1 DVDD, Camera core	2	MB_ELDO_CAM0_VCM_2P85	+2.85V Carrier Board LDO for Camera 1 VCM
3	VREG_L1F_1P2	+1.2V SOM Board power for Camera 1 DVDD, Camera core	4	GND	System Ground
5	VREG_L2F_1P2	+1.2V SOM Board power for Camera 2 DVDD, Camera core	6	MB_ELDO_CAM3_VCM_2P85	+2.85V Carrier Board LDO for Camera 4 VCM
7	MB_ELDO_CAM1_DVDD_1P1	+1.1V Carrier Board LDO for Camera 2 DVDD, Camera core	8	VREG_L5F_2P85	+2.85V SOM Board power for Camera AVDD
9	MB_ELDO_CAM0_AVDD_2P85	+2.85V Carrier Board LDO for Camera 1 AVDD	10	GND	System Ground
11	VREG_L3F_1P0	+1.0V SOM Board power for Camera 3 DVDD, Camera core	12	MB_VREG_3P3	+3.3V Carrier Board buck-boost power supply for general +3.3V rail
13	MB_ELDO_CAM2_DVDD_1P1	+1.1V Carrier Board LDO for Camera 3 DVDD, Camera core	14	MB_ELDO_CAM2_VCM_2P85	+2.8V Carrier Board LDO for Camera 3 VCM
15	MB_ELDO_CAM1_AVDD_2P85	+2.85V Carrier Board LDO for Camera 2 AVDD	16	GND	System Ground

Pin No	Signal	Description	Pin No	Signal	Description
17	MB_VREG_1P8	+1.8V Carrier Board Buck Power Supply for general +1.8V rail	18	MB_VREG_3P3	+3.3V Carrier Board buck-boost power supply for general +3.3V rail
19	MB_VREG_5P0	+5.0V Carrier Board Boost Power Supply for general +5.0V rail.	20	DC_IN_12V	Main +12.0V Power from DC power jack

3.7.7 User Buttons and LEDs (7, 36, 41, 42)

There are four user buttons and four LEDs on the Open-Q 865XR SOM Development Kit as described in the tables below. See items 7, 36, 41, 42 in Figure 1 for the carrier board locations of the user buttons and LEDs, respectively.

Table 9. Development Kit Buttons (7)

Reference Designator	User Button	Function
S2400	Volume +	Use this button to control or increase the volume.
S2402	Volume -/Reset	Use this button to control or decrease the volume. This button can also be used to reset the board.
S2401	GP User	This is a general-purpose user button connected to GPIO_117. GPIO_117 is shared with a signal on the M.2 PCIe socket (see section 3.7.16). Concurrent usage of both the user button and M.2 socket may not be possible.
S2403	Power ON	Use this button to power on the Open-Q 865XR development kit (when the auto boot configuration not enabled; see 3.7.2 above).

Table 10. Development Kit LEDs (36)

Reference Designator	LED	Function
DS2400	Blue LED	General purpose LED

Reference Designator	LED	Function
DS2401	Green LED	General purpose LED
DS2402	Red LED	General purpose LED
DS2404	Green LED	LED indicates input power
DS2403	Green LED	LED indicates boot state. This LED is controlled via GPIO_15 with is shared with the Sensor Header (see section 3.7.18).
DS2405	Green LED	LED indicates USB VBUS power

3.7.8 Debug Serial UART over USB J1500 (12)

The UART connection used on the Open-Q 865XR is a USB micro B connector (J1500). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed. Use latest FTDI drivers from https://www.ftdichip.com/FTDrivers.htm instead of system update. See item 12 in Figure 1 for the location of J1500 on the carrier board.

3.7.9 Optional Debug UART Header J1501 (9)

The UART connection used on the Open-Q 865XR is a UART header (J1501). This is an optional debug header. This debug header and J1500 should not be used at the same time. The following table describes the pinout of the debug UART header. This debug UART is available over USB via the USB to TTL Serial 1.8V cable. To get the serial terminal working with a PC. See item 9 in Figure 1 for the location of J1501 on the carrier board.

Table 11. Debug UART J1501 Pinout

Pin No	Signal	Description
1	DBG_UART_RX	UART RX signal (connect to USB to TTL Serial 1.8V cable RX)
2	DBG_UART_TX	UART TX signal (connect to USB to TTL Serial 1.8V cable TX)
3	GND	System Ground

3.7.10 USB 3.1 Type C (for ADB) J2200 (11)

The Open-Q 865XR carrier board contains one USB 3.1 Type C connection (J2200). This connection is used for Android debug bridge (ADB) functionality. To get the adb shell, ensure that the board is up and running and connect the Type C cable between the board and the PC. Type the command adb root and

adb shell on the PC prompt to exercise the adb shell functionality. While ADB utilizes only the high-speed channel, this USB type C connector supports the USB 3.1 specification including the super speed data channel. This USB connection is also uses as the charge source when the dev kit is powered by a battery and battery charging is enabled (see section 3.7.3 above). See item 11 in Figure 1 for the location of J2300 on the carrier board.

3.7.11 USB 3.1 Type A Connector J2300 (5)

The Open-Q 865XR carrier board contains one USB Type A connector J2300 situated on the north side of carrier board, which exposes USB 3.1 host functionality. This USB connection is designed to provide up to 1A VBUS current for external devices. See item 5 in Figure 1 for the location of J2300 on the carrier board.

If the user intends to use a M.2 PCIe card on the dev kit that requires a USB connection (see 3.7.15 below), then the M.2 PCIe USB enable DIP switch S2301 (6) must be switched to closed / ON (figure below). If the DIP switch is closed, the USB 3.1 Type A connector is not functional.

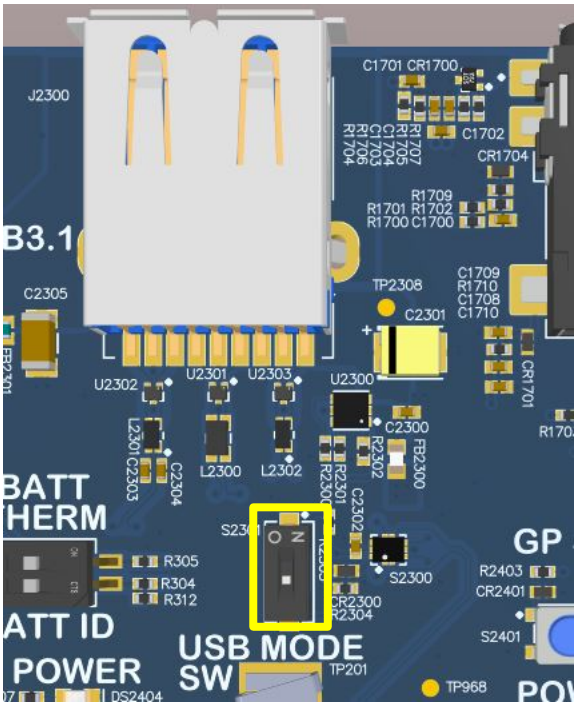

Figure 10. M.2 PCIe USB Enable DIP Switch (6)

3.7.12 Micro SD Card Socket J1400 (22)

J1400 (Micro-SD card connector) provides 4-bit secure digital (SD) interface for external storage. It is located on the bottom side of the carrier board right under the Display Module (see figure below). The SD interface supports High Speed mode.

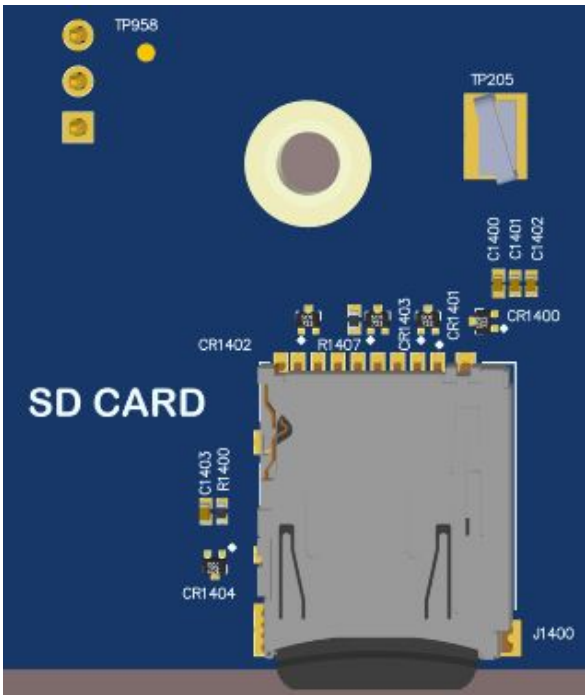

Figure 11. Micro SD Card Socket J1400

3.7.13 Display Connector J1300 (38)

The 100-pin display connector, J1300, allows for an optional display adapter to be connected to the development kit. Lantronix offers a compatible LCD panel accessory for the Open-Q 865XR SOM Development Kit. It can be purchased by contacting sales: http://www.lantronix.com/about-us/contact/.

Exposed on the display connector are the following interfaces:

- Two 4-lane MIPI DSI high speed display interfaces
- LCD backlight control signals
- I2C bus for touch panel support
- Additional GPIOs for general purposes available
- Various power rails for powering the display adapter

For details on the signal list provided on the display connector, see the development kit schematic (R-3) and the display adapter design guide technical note document (R-4).

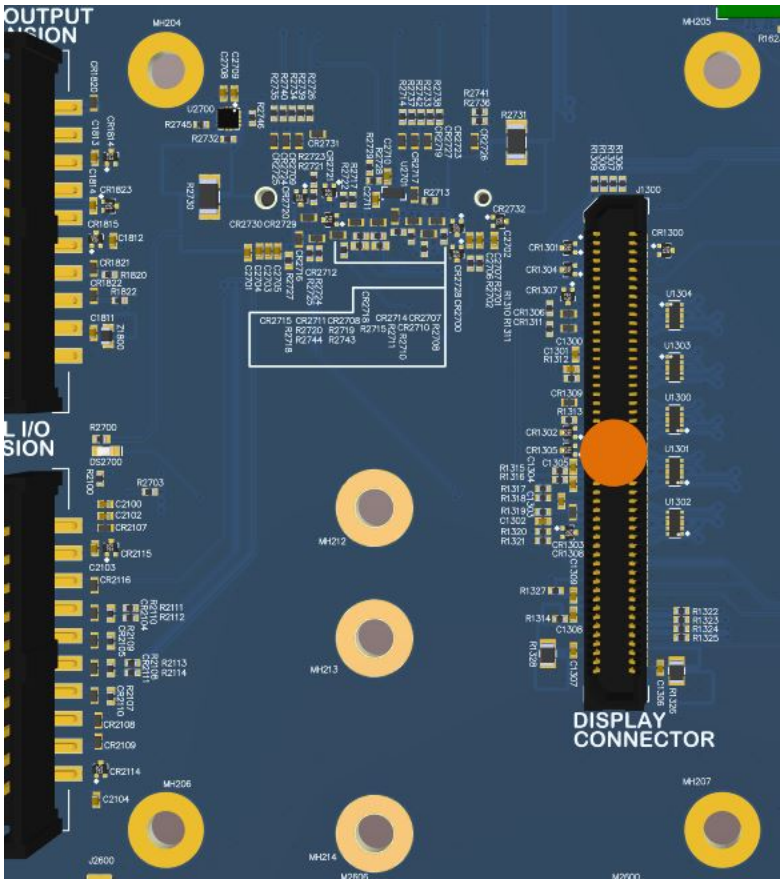

Figure 12. Display Connector J1300

3.7.14 Camera Connectors J1000 (15), J1100 (16), J1200 (17)

The Open-Q 865XR SOM Development Kit includes three camera interface connectors, J1000, J1100 and J1200 allowing users to connect multiple camera adapters to the development kit. See items 15 through 17 in Figure 1 for the carrier board locations of the camera connectors.

Lantronix offers compatible camera module accessories for the Open-Q 865XR SOM Development Kit here: https://shop.intrinsyc.com/collections/accessories

Exposed on each camera connector are the following interfaces:

- One 4-lane MIPI CSI high speed camera interface
- Camera Control Interface (CCI) I2C bus for camera and actuator control
- Additional GPIOs for general purposes available
- Various power rails for powering the camera adapter

For details on the signal list provided on the camera connectors, see the development kit schematic (R-3) and the camera adapter design guide technical note document (R-5).

3.7.15 Camera option Connectors J1001 (18), J1101 (19), J1201(20)

In addition to the three camera connectors, the video capturing subsystem of the Open-Q 865XR SOM Development Kit is equipped with three connectors for camera optional signals (J1001, J1101 and J1201). The option connector pins are NOT connected anywhere else on the CB and is expected to be connected via wires to other GPIO headers on the dev kit if desired to be used by the dev kit user.

See items 18, 19 and 20 in Figure 1 for the carrier board locations of the camera option connectors. The pinout of the connectors in shown in the table below.

Table 12. Camera option Connectors pinout

Pin No	Signal Name	Description
1	CAM_FRAME_SYNC	Camera connector pin 12 frame sync, need wires to other GPIO header
2	CAM_FLASH_TRIG	Camera connector pin 18 flash trigger, need wires to other GPIO header
3	CAM_IRQ	Camera connector pin 37 interrupt request, need wires to other GPIO header
4	GND	System Ground

3.7.16 M.2 PCIe Card Connector J2700 (24)

The Open-Q 865XR SOM Development Kit includes a M.2 PCIe socket with a B-Key ID J2700 (24) and an optional SIM card socket J2701 (25) on the bottom side of the carrier board (see image below).

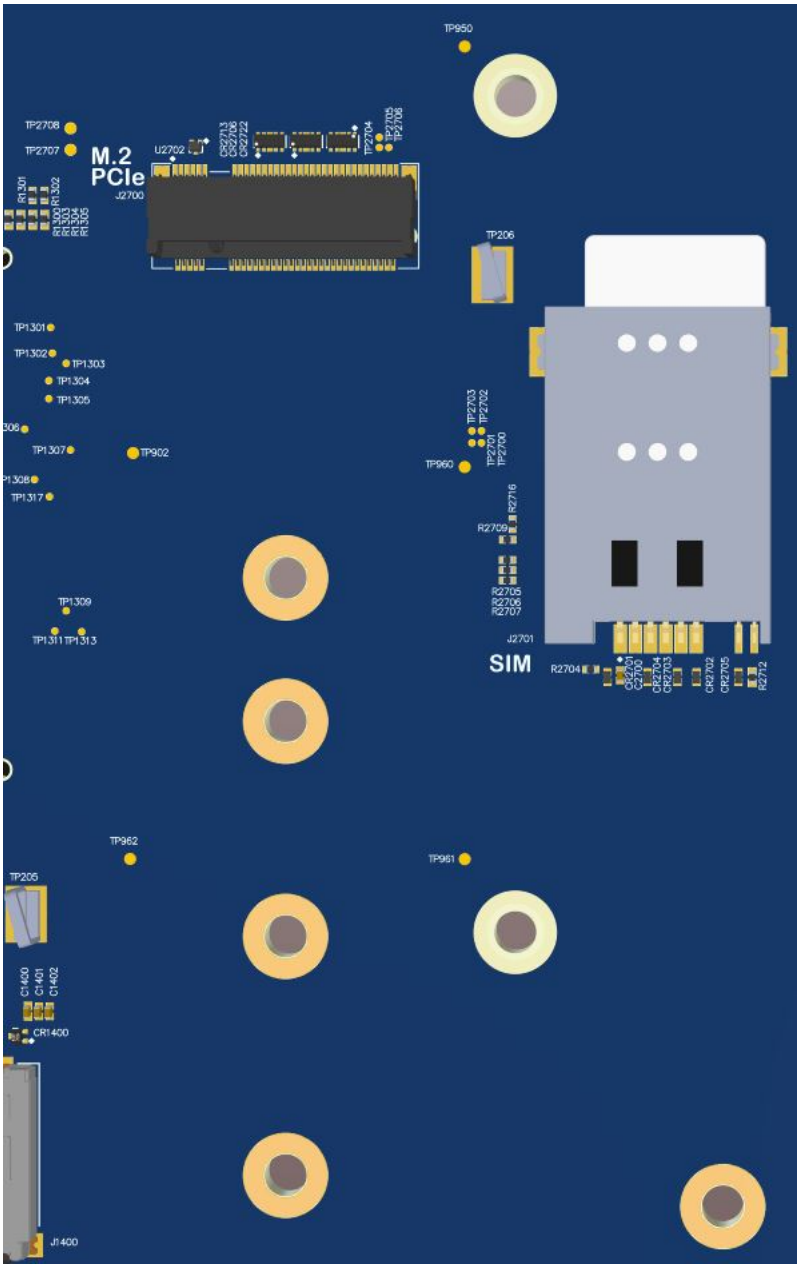

Figure 13. M.2 PCIe and Optional SIM Card Sockets

The M.2 PCIe card socket supports 30, 42, 60, and 80mm length PCI Express M.2 cards with the 4 mounting holes located below J2700 in the image above. The pinout of J2700 complies with the PCI Express M.2 card standards. Please refer to the document at the following link for more information: https://www.pcisig.com/specifications/pciexpress/base/#mini1.2

Special Notes:

- The optional SIM card socket J2701 (25) can be used if the user is connecting a M.2 PCIe card with cellular connection capabilities.
- If the user intends to use a M.2 PCIe card on the dev kit that requires a USB connection, then the M.2 PCIe USB enable DIP switch S2301 (6) must be switched to closed / ON. See Figure 6. M.2

PCIe USB Enable DIP Switch (6). If the DIP switch is closed, the USB 3.1 Type A connector J2300 (5) is not functional.

- Pin 25 of the M.2 Socket connects to GPIO_117. GPIO_117 is shared with general purpose user button (see section 3.7.7). Concurrent usage of both the user button and M.2 socket may not be possible.

3.7.17 Digital IO Expansion Header J2100 (23)

The Open-Q 865XR SOM Development Kit includes a digital IO expansion header J2100 which provides access to a selection of SOM GPIO signals and power rails. See item 23 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 13. Digital IO Expansion Header J2100 Pinout

Pin No	Signal	Description	Pin No	Signal	Description
1	No Net	No Net	2	VREG_S4A_1P8	SOM LDO Regulator S4A +1.8V
3	GPIO_41_QUP14_FP_SPI_MOSI	CPU GPIO41/QUP14	4	MB_VREG_3P3	Carrier board switching regulator. 3.3V
5	GPIO_40_QUP14_FP_SPI_MISO	CPU GPIO40/QUP14	6	PM8150L_GP10_PWM	PM8150L GPIO10
7	GPIO_43_QUP14_FP_SPI_CS	CPU GPIO43/QUP14	8	GPIO_9_QUP4_CAM_SPI1_MOSI	CPU GPIO9/QUP4
9	GPIO_42_QUP14_FP_SPI_CLK	CPU GPIO42/QUP14	10	GPIO_8_QUP4_CAM_SPI1_MISO	CPU GPIO8/QUP4
11	No Net	No Net	12	GPIO_11_QUP4_CAM_SPI1_CS0_N	CPU GPIO11/QUP4
13	GPIO_57_QUP18_SPI_MOSI	CPU GPIO57/QUP18	14	GPIO_10_QUP4_CAM_SPI1_CLK	CPU GPIO10/QUP4
15	GPIO_56_QUP18_SPI_MISO	CPU GPIO56/QUP18	16	GPIO_59_QUP18_SPI_CS_N	CPU GPIO59/QUP18
17	GND	System Ground	18	GPIO_58_QUP18_SPI_CLK	CPU GPIO58/QUP18

Pin No	Signal	Description	Pin No	Signal	Description
19	No Net	No Net	20	MB_VREG_5P0	Carrier board switching regulator +5.0V

For more details regarding configuring the GPIOs on this header, refer to the Open-Q 865XR Software Release Notes to determine feature support in the latest software release.

3.7.18 Sensor IO Expansion Header J2000 (21)

The Open-Q 865XR SOM Development Kit includes a sensor expansion header J2000 which provides a connection to an optional sensor board. If sensor functionality is not required, this header may be used for other applications. See item 21 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 14. Sensor Expansion Header J2000 Pinout

Pin No	Signal	Description	Pin No	Signal	Description
1	GPIO_170_SNS_I2C4_SDA	GPIO_170 / SSC10 (SSC4_I2C_SDA)	2	GPIO_123_IMU1_INT	GPIO123
3	GPIO_171_SNS_I2C4_SCL	GPIO_171 / SSC11 (SSC4_I2C_SCL)	4	GPIO_112_IMU2_INT	GPIO112
5	GPIO_15_RADAR_INT	GPIO15 – shared with Boot LED. See note below about usage.	6	GPIO_121_HALL_INT_N	GPIO121
7	VREG_L8C_1P8	SOM power L8C +1.8V	8	VREG_L10C_3P0	SOM power L10C +3.0V
9	GND	System Ground	10	GND	System Ground
11	GPIO_169_SNS_I2C3_SCL	GPIO_169 / SSC9	12	GPIO_162_SNS_I3C1_SDA	GPIO162/SSC2
13	GPIO_168_SNS_I2C3_SDA	GPIO168/SSC8	14	GPIO_163_SNS_I3C1_SCL	GPIO163/SSC3
15	GPIO_160_SNS_I3C0_SDA	GPIO_160 / SSC0	16	GPIO_113_MAG_INT_N	GPIO113

		(SSC0_I2C_SDA)			
17	GPIO_161_SNS_I3C0_SCL	GPIO_161 / SSC1 (SSC0_I2C_SCL)	18	GPIO_129_PRESS_INT	GPIO129
19	GPIO_167_SNS_SPI2_CS0_N	GPIO_167 / SSC7 (SSC2_SPI0_CS_0)	20	GPIO_165_SNS_SPI2_MOSI	GPIO_165 / SSC5 (SSC2_SPI0_MOSI)
21	GPIO_166_SNS_SPI2_CLK	GPIO_166 / SSC6 (SSC2_SPI0_CLK)	22	GPIO_164_SNS_SPI2_MISO	GPIO_164 / SSC4 (SSC2_SPI0_MISO)
23	GPIO_122_ALSP_INT_N	GPIO122	24	GPIO_64_SAR_INT_N	GPIO64

For more details regarding configuring the GPIOs on this header, refer to the Open-Q 865XR SOM Software Release Notes to determine feature support in the latest software release.

Special Notes:

- GPIO_15_RADAR_INT (pin 6) is shared with the Boot LED (see section 3.7.7) on the development kit. In order to use GPIO_15 on the sensor header, R2409 should be removed and software changes are needed to remove the boot LED functionality. Since the software changes are in the bootloader image, these changes need to be performed by Lantronix. See R-3 schematics for details.

3.7.19 Audio Inputs Expansion Header J1800 (27)

The Open-Q 865XR SOM Development Kit audio subsystem is built around the Qualcomm Audio Codec WCD9385 (28). The Audio Inputs Expansion Header J1800 exposes some of the audio input capabilities of WCD9385 for the user. See item 27 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 15. Audio Inputs Expansion Header Pinout J1800

Pin No	Signal	Description	Pin No	Signal	Description
1	CDC_IN1_P	Codec Input 1 Positive	2	CDC_IN1_N	Codec Input 1 Negative
3	CDC_IN6_P	Codec Input 6 Positive	4	CDC_IN6_N	Codec Input 6 Negative
5	CDC_MIC_BIAS1	Microphone Bias 1	6	CDC_MIC_BIAS3	Microphone Bias 3
7	CDC_IN7_P	Codec Input 7 Positive	8	CDC_IN7_N	Codec Input 7 Negative

Pin No	Signal	Description	Pin No	Signal	Description
9	CDC_MIC_BIAS4	Microphone Bias 4	10	MB_VREG_3P3	Carrier board switching regulator +3.3V
11	GND	System Ground	12	GND	System Ground
13	CDC_DMIC_CLK3	Digital Microphone 3 Clock	14	CDC_DMIC_CLK4	Digital Microphone 4 Clock
15	CDC_DMIC_DATA 3	Digital Microphone 3 Data	16	CDC_DMIC_DATA 4	Digital Microphone 4 Data
17	VREG_S4A_1P8	SOM LDO Regulator S4A +1.8V	18	CDC_DMIC_CLK5	Digital Microphone 5 Clock
19	GND	System Ground	20	CDC_DMIC_DATA 5	Digital Microphone 5 Data

3.7.20 Audio Outputs Expansion Header J1801 (26)

The Open-Q 865XR SOM Development Kit audio subsystem is built around the Qualcomm Audio Codec WCD9385 (28). The Audio Outputs Expansion Header J1801 exposes some of the audio output capabilities of WCD9385 for the user. See item 26 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 16. Audio Outputs Expansion Header Pinout J1801

Pin No	Signal	Description	Pin No	Signal	Description
1	CDC_LINE_OUT1_P	Codec Line Out 1 Positive	2	CDC_LINE_OUT1_N	Codec Line Out 1 Negative
3	No Net	No Net	4	No Net	No Net
5	CDC_LINE_REF	Codec Reference (GND)	6	MB_VREG_3P3	Carrier board switching regulator +3.3V
7	No Net	No Net	8	No Net	No Net
9	CDC_EAR_P	Earphone Amplifier Output Positive	10	CDC_EAR_N	Earphone Amplifier Output Negative
11	GND	System Ground	12	SOM_SYS_PWR_PER	SOM System Power
13	CDC_SWR_CLK	Codec PDM Clock	14	CDC_SWR_DATA	Codec PDM Data
15	CDC_WSA_EN	SOM PMIC GPIO127, can be used as	16	CDC_WSA_EN2	SOM PMIC GPIO128, can be used as

Pin No	Signal	Description	Pin No	Signal	Description
		Speaker Amp Enable 2			Speaker Amp Enable 2
17	VREG_S4A_1P8	SOM LDO Regulator S4A +1.8V	18	DC_IN_12V	Voltage from DC Power Input +12.0V
19	MB_VREG_5P0	Carrier board switching regulator +5.0V	20	GND	System Ground

For more details regarding configuring the GPIOs on this header, refer to the Open-Q 865XR Software Release Notes to determine feature support in the latest software release.

3.7.21 Audio IO Expansion Header J1900 (10)

In addition to the Qualcomm Audio Codec WCD9385 (28), the Open-Q 865XR SOM Development Kit also includes other digital audio interfaces. The Audio IO Expansion Header J1900 exposes some of these interfaces for the user. See item 10 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 17. Audio IO Expansion Header Pinout J1900

Pin No	Signal	Description	Pin No	Signal	Description
1	GPIO_152_LPI_MI2S1_CLK_R	CPU GPIO152 – can be configured as LPI_MI2S1_MCLK	2	GND	System Ground
3	GPIO_153_LPI_MI2S1_WS	CPU GPIO153 – can be configured as LPI_MI2S1_SCK	4	GPIO_133_MI2S2_I2S_SCK_R	CPU GPIO133 – can be configured as MI2S_I2S_SCK
5	GPIO_154_LPI_MI2S1_DATA0_R	CPU GPIO154 – can be configured as LPI_MI2S1_DATA0	6	GPIO_135_MI2S2_I2S_WS_R	CPU GPIO135 – can be configured as MI2S2_I2S_WS
7	GPIO_155_LPI_MI2S1_DATA1	CPU GPIO155 – can be configured as LPI_MI2S_DATA1	8	GPIO_134_MI2S2_I2S_DATA0_R	CPU GPIO134 – can be configured as MI2S_I2S_DATA0
9	GND	System Ground	10	GPIO_137_MI2S2_I2S_DATA1_R	CPU GPIO137 – can be configured as MI2S_I2S_DATA1

Pin No	Signal	Description	Pin No	Signal	Description
11	GPIO_146_LPI_MI2S0_CLK	CPU GPIO146 – can be configured as LPI_MI2S0_SCK	12	GND	System Ground
13	GPIO_147_LPI_MI2S0_WS	CPU GPIO147 – can be configured as LPI_MI2S0_WS	14	GPIO_156_LPI_MI2S2_CLK	CPU GPIO156 – can be configured as LPI_MI2S_CLK
15	GPIO_148_LPI_MI2S0_DATA0	CPU GPIO148 – can be configured as LPI_MI2S0_DATA0	16	GPIO_157_LPI_MI2S2_WS	CPU GPIO157 – can be configured as LPI_MI2S_WS
17	No Net	No Net	18	GPIO_158_LPI_MI2S2_DATA0_R	CPU GPIO158 – can be configured as LPI_MI2S_DATA0
19	GND	System Ground	20	GPIO_159_LPI_MI2S2_DATA1_R	CPU GPIO159 – can be configured as LPI_MI2S_DATA1
21	GPIO_149_LPI_MI2S0_DATA1	CPU GPIO149 – can be configured as LPI_MI2S0_DATA1	22	GND	System Ground
23	GPIO_150_LPI_MI2S0_DATA2	CPU GPIO150 – can be configured as LPI_MI2S0_DATA2	24	GPIO_4_QUP1_NFC_I2C_SDA	CPU GPIO4 – can be configured as QUP1_NFC_I2C_SDA
25	GPIO_151_LPI_MI2S0_DATA3	CPU GPIO151 – can be configured as LPI_MI2S0_DATA3	26	GPIO_5_QUP1_NFC_I2C_SCL	CPU GPIO5 – can be configured as QUP1_NFC_I2C_SCL
27	No Net	No Net	28	CDC_GPIO_0	WCD9385 Audio Codec GPIO0
29	GND	System Ground	30	CDC_GPIO_1	WCD9385 Audio Codec GPIO1
31	MB_VREG_1P8	Carrier board switching regulator +1.8V	32	GND	System Ground
33	MB_VREG_3P3	Carrier board switching regulator +3.3V	34	RED_LED	RED LED
35	MB_VREG_5P0	Carrier board switching regulator +5.0V	36	GREEN_LED	GREEN LED
37	DC_IN_12V	Voltage from DC Power Input +12.0V	38	BLUE_LED	BLUE LED

Pin No	Signal	Description	Pin No	Signal	Description
39	GND	System Ground	40	No Net	No Net

1. Population option changes are necessary in order to use this signal. See the carrier board schematic (R-3) for more details.

For more details regarding configuring the GPIOs on this header, refer to the Open-Q 865XR Software Release Notes to determine feature support in the latest software release.

3.7.22 Audio Headset Jack J1700 (8)

In addition to the audio expansion headers, the Open-Q 865XR SOM Development Kit also includes a standard 3.5mm audio headset jack J1700, which provides connection to headphone, microphone input and headset detection circuits. See item 8 in Figure 1 for the carrier board location of this headset jack.

3.7.23 WLAN / BT Antenna Connections (13, 14)

The Open-Q 865XR SOM Development Kit WLAN/BT functionality is based on Qualcomm QCA6391 chipset. It provides WLAN/Bluetooth in 2x2 MIMO with two spatial streams IEEE802.11 a/b/g/n/ac/ax WLAN standards, and Bluetooth + LE 5.x + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.

The QCA6391 chipset is located on the SOM, which has U.FL coax connectors for channel 0 (WLAN+BT) and channel 1 (WLAN only). These connectors are mated to the Carrier board WLAN / BT PCB antennas via coax cables. Figure 1 in 3.4.1 above shows how the two WLAN / BT are routed via the coax cables:

- For channel 0 (WLAN+BT), see items 31 and 13 on Figure 1.
- For channel 1 (WLAN only), see items 32 and 14 on Figure 1.

If a more advanced antenna solution is required, it is possible to connect custom antennas directly to the SOM U.FL connectors.

3.7.24 Quiet Thermistor RT800 (34)

The Open-Q 865XR SOM Development Kit includes a thermistor on the carrier board to allow for system level thermal management. See item 34 in Figure 1 for the carrier board location of the Quiet Thermistor RT800.