LANTRONIX® Formerly INTRINSYC

Open-Q™ 845 µSOM Development Kit User Guide

Part Number PMD-00015

Revision A July 2020

Contacts

Lantronix, Inc.
7535 Irvine Center Drive, Suite 100
Irvine, CA 92618, USA
Toll Free: 800-526-8766
Phone: 949-453-3990
Fax: 949-453-3995

IES Customer Support Portal
https://helpdesk.intrinsyc.com

Lantronix Technical Support
http://www.lantronix.com/support

Sales Offices
For a current list of our domestic and international sales offices, go to the Lantronix web site at http://www.lantronix.com/about-us/contact/

Revision History

Date	Rev.	Comments
October 2019	1.0	Initial release October 7, 2019 Document title: Open-Q 845 µSOM Development Kit User Guide Intrinsyc document number: ITC-01DEV1430-UG-001
July 2020	A	Initial Lantronix document. Added Lantronix document part number, Lantronix logo, branding, contact information, and links.

For the latest revision of this product document, please go to: http://tech.intrinsyc.com.

Table of Contents

List of Figures

List of Tables

1 Introduction

1.1 Purpose

The purpose of this user guide is to provide instructions and technical information on the Open-Q 845 µSOM Development Kit.

You can find information on this and other Lantronix development kits on the Lantronix web site: http://www.lantronix.com/products

1.2 Scope

This document will cover the following items on the Open-Q 845 µSOM Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- SOM
- Carrier Board
- Available peripherals

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Lantronix Open-Q 845 µSOM Development Kit.

2 Documents

This section lists the supplementary documents for the Open-Q 845 µSOM Development Kit.

2.1 Applicable Documents

REFERENCE	TITLE
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.2 Reference Documents

The below listed documents are available on the Technical Portal: https://tech.intrinsyc.com (dev kit registration required)

REFERENCE	TITLE
R-1	Open-Q 845 µSOM Datasheet
R-2	Open-Q 845 µSOM – Carrier Board Design Guide
R-3	Open-Q 845 µSOM Schematics (SOM and Carrier)
R-4	Open-Q 845 µSOM Development Kit – Display Adapter Design Guide
R-5	Open-Q 845 µSOM Development Kit – Camera Adapter Design Guide
R-6	Open-Q 845 µSOM Development Kit – Battery Charging Tech Note

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array

GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
QUP	Qualcomm Universal Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SOM	System on Module
SPMI	System Power Management Interface (Qualcomm PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

3 Open-Q 845 µSOM Development Kit

3.1 Introduction

The Open-Q 845 provides a quick reference and evaluation platform for the Qualcomm Snapdragon SDA845 Platform. The development kit is suited for Android application developers, OEMs, consumer manufacturers, hardware component vendors, camera vendors, and product designers to evaluate, optimize, test and deploy applications that can utilize the Qualcomm Snapdragon SDA845 Platform technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at

http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 845 µSOM Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap.

3.4 Development Kit Contents

The Open-Q 845 µSOM Development Kit comes with Android software pre-programmed and includes the following:

  - Open-Q 845 µSOM with the Snapdragon 845 (SDA845) processor
  - Mini-ITX form-factor carrier board

- AC power adapter

3.4.1 Important Locations

The diagram below shows the locations of key components, interfaces, and controls.

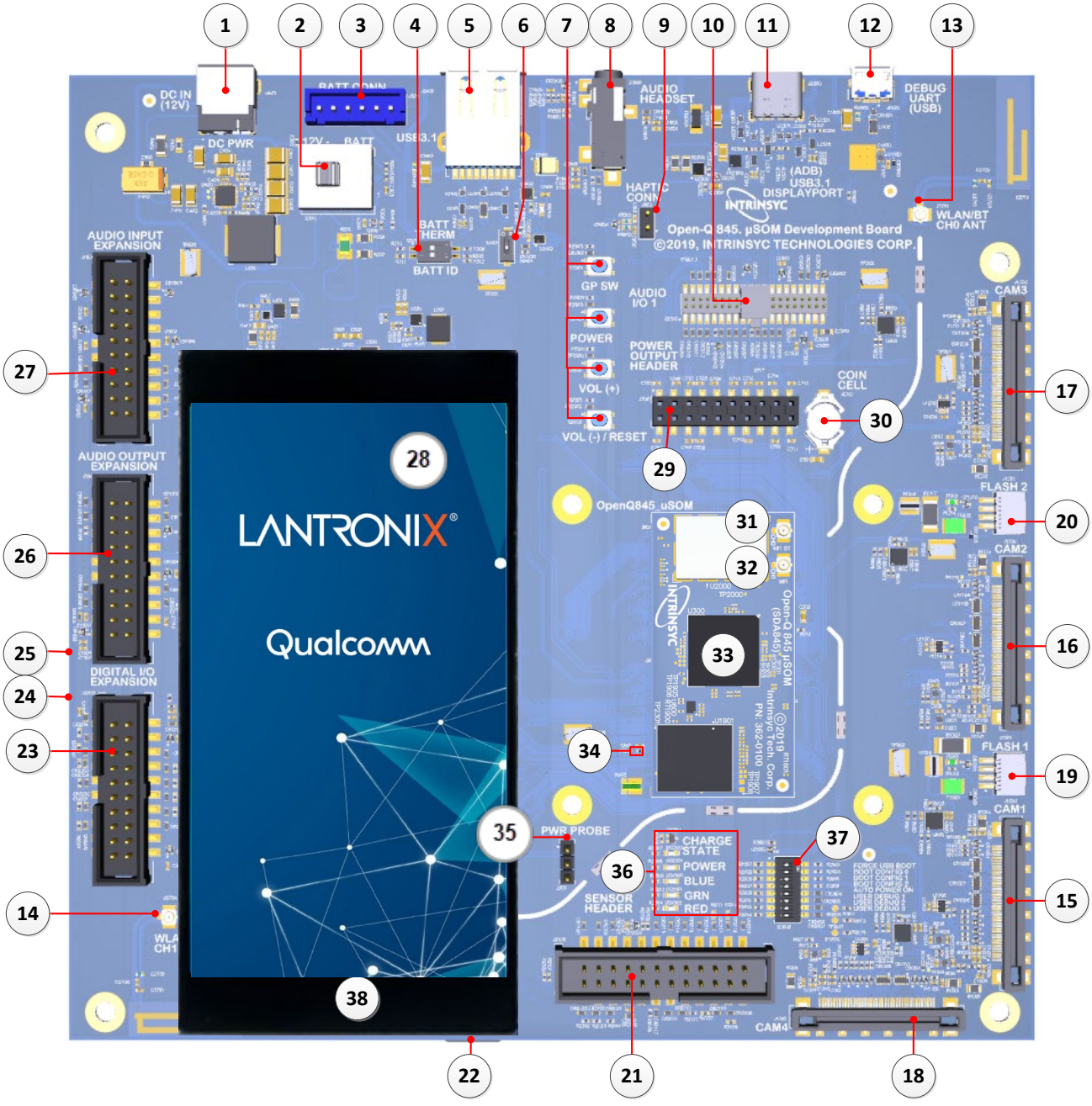

Figure 1. Assembled Open-Q 845 µSOM Development Kit

Table 1. List of Development Kit Features itemized in the figure above

Position	Feature Description	Reference Designator
1	DC Power Supply Jack	J400
2	Power Source Selector	S300
3	Battery Input Header	J300
4	Battery Configuration DIP Switch	S301
5	USB 3.1 Type A Connector	J2400
6	Mini-PCIe USB Enable DIP Switch	S2401
7	Buttons: General Purpose / Power / Volume Up / Volume Down	S2501 / S2503 / S2500 / S2502
8	Audio Headset Jack	J1800
9	Haptic Motor Header	J802
10	Audio I/O Header	J2000
11	USB 3.1 Type-C connector for ADB	J2300
12	USB Serial Debug Console	J1600
13	WLAN/BT Channel 0 External Antenna Connector	J2701
14	WLAN Channel 1 External Antenna Connector	J2700
15	Camera 1 Connector	J1000
16	Camera 2 Connector	J1100
17	Camera 3 Connector	J1200
18	Camera 4 Connector	J1300
19	Flash 1 Header	J1001
20	Flash 2 Header	J1201
21	Sensors Expansion Header	J2100
22	Micro SD card socket (on bottom side of Carrier Board)	J1500
23	Digital IO Expansion Header	J2200
24	Mini-PCIe Card Connector (on bottom side of Carrier Board)	J2801
25	SIM Card Socket for Mini-PCIe (on bottom side of Carrier Board)	J2800
26	Audio Outputs Expansion	J1901
27	Audio Inputs Expansion	J1900

28	Audio Codec Module (on top side of Carrier Board underneath Display Adapter)	U1700
29	Power Header	J700
30	Coin Cell Holder	B300
31	Open-Q 845 µSOM, WLAN/BT CH0 Antenna Connector	J2200 (on µSOM)
32	Open-Q 845 µSOM, WLAN CH1 Antenna Connector	J2201 (on µSOM)
33	Open-Q 845 µSOM	
34	On-Board Quiet Thermistor	RT800
35	SOM Current Sense Probe Header	J301
36	LEDs: (Charge State / Power / Blue / Green / Red)	DS2503 / DS2504 / DS2500 / DS2501 / DS2502
37	System Configuration DIP Switch	S2600
38	Open-Q LCD Panel	

3.4.2 Block Diagram

The block diagram below shows the connectivity and major components of the Open-Q 845 µSOM Development Kit.

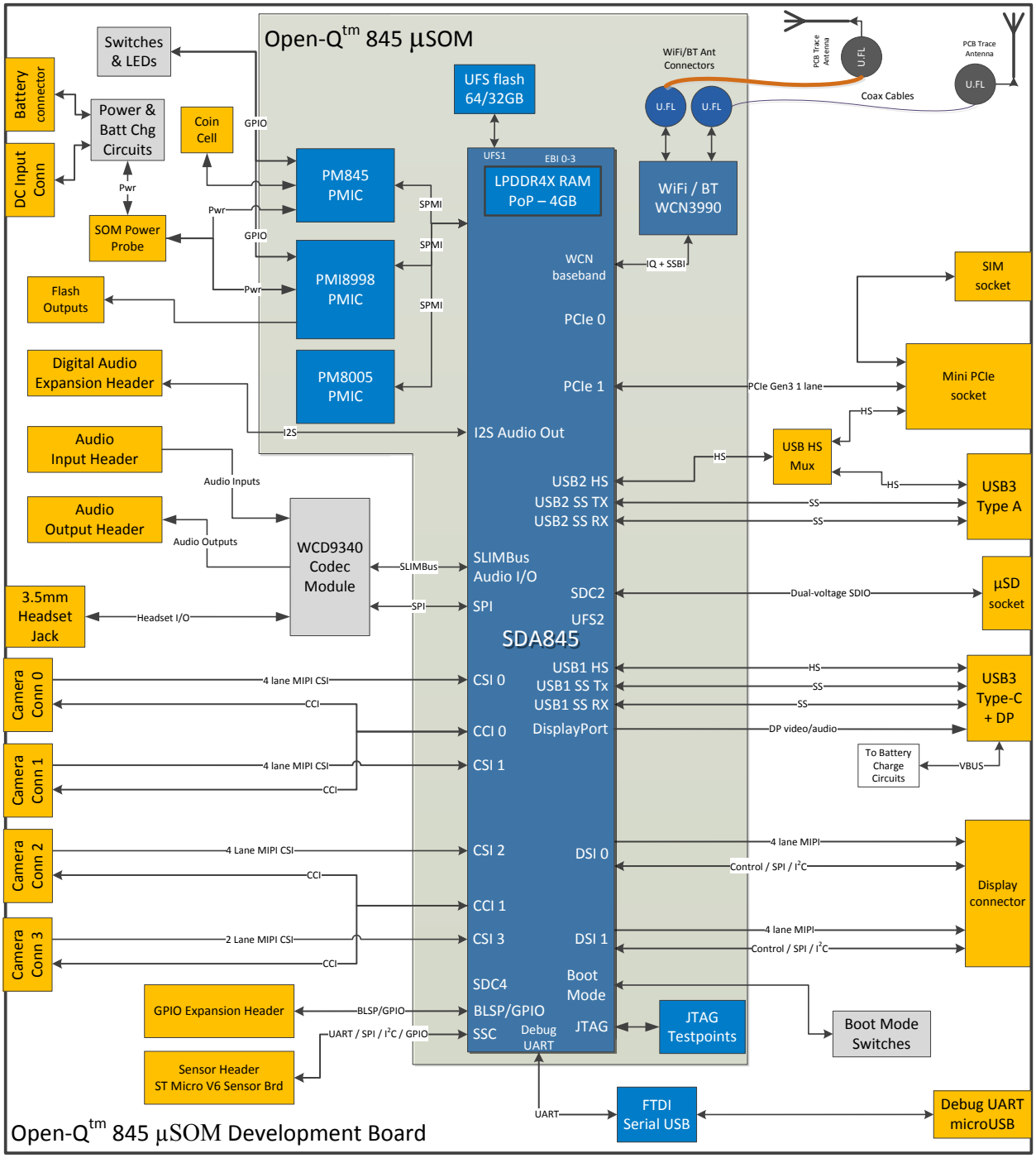

Figure 2. Open-Q 845 µSOM Dev Kit Block Diagram

3.4.3 Optional Accessories

Optional accessories are available for the Open-Q 845 µSOM Development Kit, like LCD Panel, Camera adapter, and sensor board. Please visit the product store for availability of these accessories: https://shop.intrinsyc.com/collections/accessories, or contact Lantronix Sales.

3.5 Getting Started

This section explains how to setup the Open-Q 845 µSOM Development Kit and start using it.

3.5.1 Registration

To register the development kit and gain access to the Intrinsyc Technical Document Portal, please visit: http://tech.intrinsyc.com/account/register.

To proceed with registration, the development kit serial number is required. These serial numbers can be found on the labels that are present on the SOM and carrier boards. The labels contain the following information:

- SOM: Serial Number, WIFI MAC address
- Carrier: Serial Number

Note: Please retain the SOM and carrier board serial numbers for warranty purposes.

Refer to http://tech.intrinsyc.com/account/serialnumber for more details about locating the development kit serial number.

3.5.2 Configuration Switch Settings

The default configuration for the system configuration DIP switch S2600 is for all switches to be open or OFF. For details about other configurations, see section 3.7.2.

3.5.3 Powering Up the Development Kit

The development kit can be powered up by either using a DC power supply or by connecting a battery on connector J300. Select the desired power source using the switch S300 on the carrier board. The green LED DS2504 marked “POWER” on the board is the power LED and should glow once the development kit is powered. To see the debug logs, connect a serial debug cable to the J1600 connector.

To power-up the board, perform the following exact steps below detailed below:

1. At a static-safe workstation, remove the development kit board carefully from the anti-static bag.
2. Connect the Power Adapter to the 12V DC Jack J400 and then press and hold the power button until you see the company logo appears on the on-board display (~3 seconds).
3. Navigate using the touchscreen on the on-board display.

3.6 Open-Q 845 µSOM

The Open-Q 845 µSOM contains the core Snapdragon 845 architecture. Measuring in at 50mm x 25mm, the SOM is where all the processing occurs. It is connected to the carrier board via three 100 pin Hirose DF40 connectors which allows essential power rails and signals to be exposed for supporting other peripherals and interfaces on the platform.

For detailed information about the Open-Q 845 µSOM, see the device specification noted as reference document R-1.

3.7 Open-Q 845 Carrier Board

The Open-Q 845 Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals. The table and sections below provide in depth information on the carrier board properties, user interfaces, connectors, and expansion headers found on the carrier board. This information is important for users wishing to connect other external hardware devices to the Open-Q 845 µSOM Development Kit. Users must ensure that before connecting any hardware device to the development kit, that it is compatible with the Open-Q 845 hardware specifications. See Figure 1 for position on carrier board.

Table 2. Carrier Board Features

Item	Position	Description	Specification	Usage
Form Factor		Dimensions: 170mm x 170mm	Mini-ITX Form Factor	
SOM Interface	33	3 x 100-pin Hirose DF40 connectors	SOM power and signal IO connection to carrier board.	The Open-Q 845 SOM connects to the carrier board through this interface.
Power	1	AC / Barrel charger	12 V DC Power Supply	Power Supply
Power	3	Battery connector for single cell lithium battery		Input power option
Debug Serial via USB	12	Debug Serial UART console over USB for development	USB Micro B connector	Development Serial Connector for debug output via USB
Buttons	7	General Purpose SW button	SMD Button	Additional button for general purpose
	7	Power Button	SMD Button	Power Button for Suspend / Resume and Power off
Volume Keys	7	Volume + key	SMD Button	Volume +Key
	7	Volume – key	SMD Button	Volume – Key
Sensor Connector	21	24 pin Sensor Expansion Connector		Available via Lantronix optional accessories kit
Digital IO Expansion Header	23	Exposes general purpose IO for user development		
Audio Headset Jack	8	Audio Headset Jack		Audio Headset

Item	Position	Description	Specification	Usage
Audio Inputs Expansion	27	Audio Inputs Header	3 Analog Differential Inputs, 3 PDM Input Interfaces with phantom power	Microphones
Audio Outputs Expansion	26	Audio Outputs Header	2 Line outputs, 1 earphone amplifier output, 1 Soundwire interface	Amplifiers
Audio I/O	10	Audio I/O headers	3 x I2S, 1x Analog Differential Input	Various audio I/O functions
Haptic motor header	9	Haptic device driver	LRM and ERA capable output driver	Haptic motor
Micro SD (on bottom)	22	Micro SD card	4bit Micro SD card support	External Storage
USB Type C	11		USB 3.1 type C connector	For USB debugging and client / host mode
USB Type A	5		Female Type A Connector	USB 3.1 Host interface
WLAN Antennas	13, 14	2 PCB Antennas		Coax connection to SOM WiFi module
Coin Cell Holder	30	Coin Cell battery holder provided	for PMIC RTC	
LEDs	36	Five LEDs	Three user driven LEDs	
LCD Display and Touch connector	38	100 pin for LCD signals	2x 4-lane MIPI DSI MIPI Alliance Specification for DPHY v1.2	For connecting display accessory
CSI Camera connectors	15, 16, 17, 18	4x camera connectors	MIPI Alliance Specification for CSI-2 v1.3	For connecting camera accessories.
Flash driver	19, 20	2 x Flash drivers	Low current flash driver control	Flash control
Current Sense Header	35	3 pin header	Sense lines connected across 0.005 Ohm resistor	To measure current consumption of SOM
Mini PCI Express Connector (on bottom)	24	Mini PCI Express for external peripheral connectivity	PCI Express Gen3 interface. Can support half or full size card	For external mini PCIe card
WWAN SIM Card (on bottom)	25	WWAN SIM card connector (optional)		For WWAN mini PCI express cards

3.7.1 SOM Board to Board Connectors (33)

The Open-Q 845 µSOM connects to the carrier board via three 100 pin Hirose DF40 connectors which allows essential power rails and signals to be exposed for supporting other peripherals and interfaces on the platform. For the list of signals exposed by the SOM, see the device specification (Ref. R-1).

3.7.2 Boot Configuration DIP Switch S2600 (37)

There is a DIP switch S2600 on the top side of the Open-Q 845 carrier board. The 8-bit switch allows the user to control the system configuration and boot options. The image below shows the DIP switch assignments.

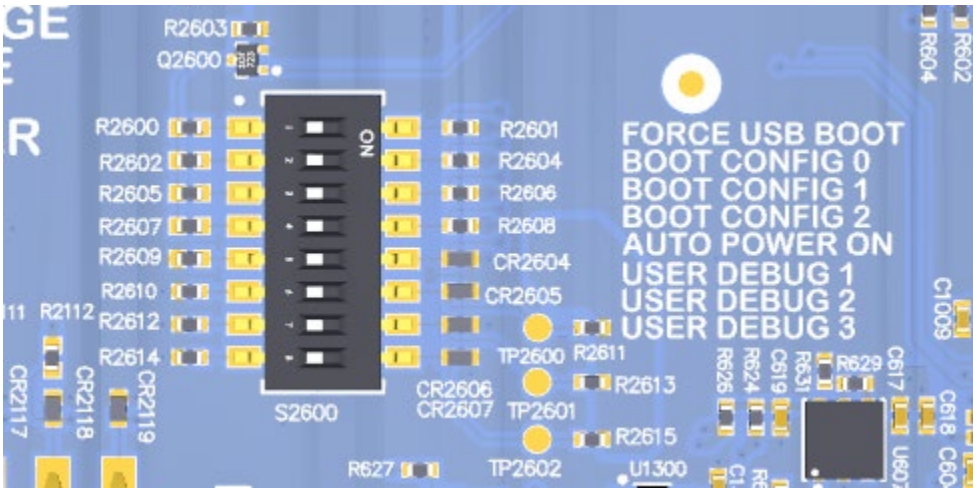

Figure 3. DIP switch assignments

See the table below for a description of the DIP switch connections.

Table 3 - Boot Configuration DIP Switch Settings

Function	DIP Switch	Description	Notes
FORCED_USB_BOOT	S2600-1	For factory mode programming. Connected to CPU GPIO57.	For Lantronix use only. Leave open / OFF.
WATCHDOG _DISABLE	S2600-2	Enables WATCHDOG_DISABLE when DIP switch turned on. Connected to CPU GPIO101	Unsupported feature. Leave switch open / OFF.
BOOT_CONFIG[1]	S2600-3	CPU boot configuration bit 1. Connected to CPU GPIO99	For default boot configuration, leave open / OFF. Other boot configurations not supported.
BOOT_CONFIG[2]	S2600-4	CPU boot configuration bit 2. Connected to CPU GPIO100	For default boot configuration, leave open / OFF. Other boot configurations not supported.
CBL_PWR_N	S2600-5	Controls the auto boot of the SOM when power is applied.	Default configuration is open / OFF. To enable auto boot of the SOM when power is applied, set switch closed / ON.
USR_DEBUG 1	S2600-6	User debug switch connected to test point TP2600.	Default out of the box configuration is OFF
USR_DEBUG 2	S2600-7	User debug switch connected to test point TP2601.	Default out of the box configuration is OFF
USR_DEBUG 3	S2600-8	User debug switch connected to test point TP2602.	Default out of the box configuration is OFF

3.7.3 Input Power Selection

The development kit can be powered using either external DC power supply or by using a battery. The input power source selection is performed by using the connectors and selection switches shown in the figure and subsections below.

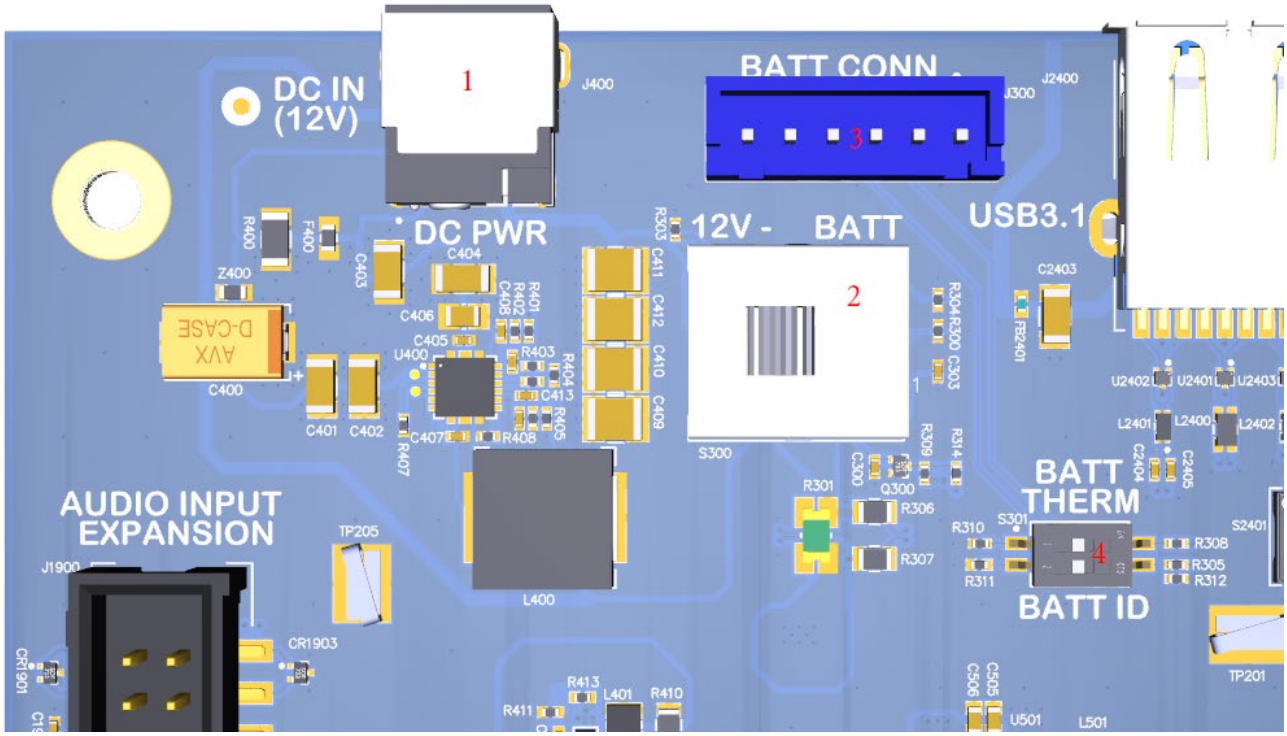

Figure 4. Input Power Selection Locations

3.7.3.1 Input Power Selection Switch S300 (2)

The S300 switch shown in the figure above is used to select the power source. To select the external DC power supply as the power source, slide the switch towards the '12V' position. To power up the kit using the battery, slide the switch towards the 'BATT' position. The default position is '12V'.

3.7.3.2 Battery ID and Thermistor Configuration DIP Switch S301 (4)

The 2-position DIP switch S301 shown in the figure above configures the battery ID and thermistor settings. The table below describes the settings for the battery ID / thermistor DIP switch.

Table 4 – Battery ID / Thermistor Configuration DIP Switch Settings

Function	DIP Switch	Description	Notes
BATTERY THERMISTOR	S301-1	Selects whether or not a 10K ohm thermistor is attached to the battery connector J300.	For DC powered dev kit, set switch to closed / ON (default). This enables the

Function	DIP Switch	Description	Notes
			use of the 'fake' 10K thermistor on the carrier board. For battery powered dev kit, set switch to open / OFF if thermistor is included on the battery pack. Otherwise keep switch closed / ON.
BATTERY ID	S301-2	Informs the 845 µSOM whether a valid battery is connected. The setting is used as input to enable or disable battery charging.	For DC power dev kit, set switch to closed / ON (default) to disable battery charging. For battery power dev kit, set switch to open / OFF to enable battery charging.

3.7.3.3 DC Power Input Jack J400 (1)

For a DC powered Open-Q 845 µSOM Development Kit, the DC power input jack J400 (see location in figure above) is used to connect to the include +12V DC power supply. The 845 carrier board includes circuitry to convert the +12V input into different voltage rails that are needed by 845 µSOM and carrier board peripherals.

3.7.3.4 Battery Connector J300 (3)

For a battery powered Open-Q 845 µSOM Development Kit, the battery connector J300 (see location in figure above) is used for connection to the battery. The table below describes the pinout of the battery connector. For more information on powering the development kit from a battery, including selecting a battery pack, see reference document R-6.

Table 5. Battery Connector J300 Pinout

Pin No	Signal	Description
1	GND	System ground, Battery Negative Wire
2	GND	System ground, Battery Negative Wire
3	BATT_THERM_CONN	10K Thermistor
4	BATT_ID_CONN	ID Resistor (optional)
5	VBATT_CONN	Battery Positive Wire
6	VBATT_CONN	Battery Positive Wire

3.7.4 SOM Current Sense Header J301 (35)

The SOM Current Sense header, J301, can be used to monitor the SOM's current consumption on the main SOM_SYS_PWR power rail. A close up of the J301 (PWR PROBE) location is shown below.

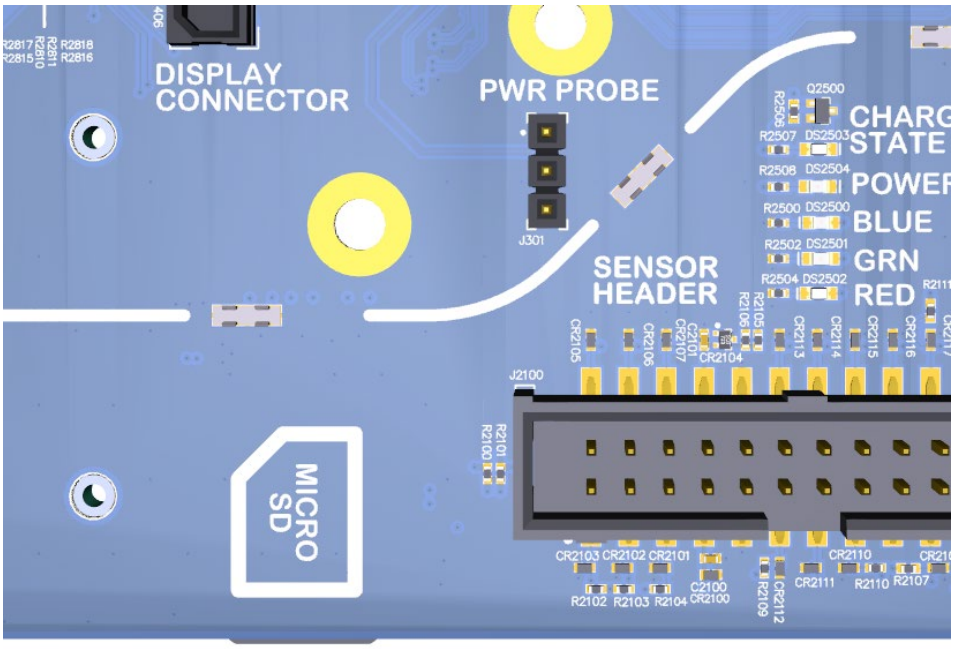

Figure 5. SOM Current Sense Header J301 (5)

The table below summarizes the pin outs of header J301

Table 6 - Power Header J301 Pinout

Pin No	Signal	Description
1	SOM_PWR_SENSE_P	SOM power positive current sense line
2	SOM_PWR_SENSE_N	SOM power negative current sense line
3	GND	System Ground

To obtain power consumption measurements, the header is connected to a data acquisition unit (Keithley 2701 or similar) and the voltages on the SOM_PWR_SENSE_P/N pins are captured a few times a second over the test period (typically 30 minutes). The SOM power consumption is then calculated as (where Rsense = 5 milliohms):

$$Psom = Vsom_{pwr_{sense_N}} * \frac{(Vsom_{pwr_{sense_P}} - Vsom_{pwr_{sense_N}})}{Rsense}$$

Use averaging to reduce noise.

3.7.5 Coin Cell Battery Holder B300 (30)

The coin cell holder allows the user to use a coin cell for supplying power to the SOM VCOIN power input. It is recommended that the Panasonic ML621 series rechargeable coin cell be used (not supplied with the development kit). See item 30 in Figure 1 for the coin cell battery holder location on the 845 carrier board.

3.7.6 Power Header J700 (36)

The Power Header J700 provides access to various carrier board voltage rails. The pinout of the connector is listed in table below. See item 36 in Figure 1 for the power header location on the 845 carrier board.

Table 7. Power Header J700 (36)

Pin No	Signal	Description	Pin No	Signal	Description
1	MB_ELDO_CAM0_DVDD_1P1	+1.1V Carrier Board LDO for Camera 1 DVDD, Camera core	2	MB_ELDO_CAM0_VCM_2P85	+2.85V Carrier Board LDO for Camera 1 VCM
3	MB_ELDO_CAM3_DVDD_1P1	+1.1V Carrier Board LDO for Camera 4 DVDD, Camera core	4	GND	System Ground
5	MB_VREG_1P8	+1.8V Carrier Board Buck Power Supply for general +1.8V rail	6	MB_ELDO_CAM3_VCM_2P85	+2.85V Carrier Board LDO for Camera 4 VCM
7	MB_ELDO_CAM1_DVDD_1P1	+1.1V Carrier Board LDO for Camera 2 DVDD, Camera core	8	MB_ELDO_CAM1_VCM_2P85	+2.8V Carrier Board LDO for Camera 2 VCM
9	MB_ELDO_CAM0_AVDD_2P85	+2.85V Carrier Board LDO for Camera 1 AVDD	10	GND	System Ground
11	MB_VREG_1P8	+1.8V Carrier Board Buck Power Supply for general +1.8V rail	12	MB_VREG_3P3	+3.3V Carrier Board buck-boost power supply for general +3.3V rail
13	MB_ELDO_CAM2_DVDD_1P1	+1.1V Carrier Board LDO for Camera 3 DVDD, Camera core	14	MB_ELDO_CAM2_VCM_2P85	+2.8V Carrier Board LDO for Camera 3 VCM
15	MB_ELDO_CAM1_AVDD_2P85	+2.85V Carrier Board LDO for Camera 2 AVDD	16	GND	System Ground
17	MB_VREG_1P8	+1.8V Carrier Board Buck Power Supply for general +1.8V rail	18	MB_VREG_3P3	+3.3V Carrier Board buck-boost power supply for general +3.3V rail

Pin No	Signal	Description	Pin No	Signal	Description
19	MB_VREG_5P0	+5.0V Carrier Board Boost Power Supply for general +5.0V rail.	20	DC_IN_12V	Main +12.0V Power from DC power jack

3.7.7 User Buttons and LEDs (7, 36)

There are four user buttons and four LED's on the Open-Q 845 µSOM Development Kit as described in the tables below. See items 7 and 36 in Figure 1 for the carrier board locations of the user buttons and LEDs, respectively.

Table 8. Development Kit Buttons (7)

Reference Designator	User Button	Function
S2500	Volume +	Use this button to control or increase the volume.
S2502	Volume -/Reset	Use this button to control or decrease the volume. This button can also be used to reset the board.
S2501	GP Switch	This is a general-purpose user button.
S2503	Power ON	Use this button to power on the Open-Q 845 development kit (when the auto boot configuration not enabled; see 3.7.2 above).

Table 9. Development Kit LEDs (36)

Reference Designator	LED	Function
DS2500	Blue LED	General purpose LED
DS2501	Green LED	General purpose LED
DS2502	Red LED	General purpose LED
DS2504	Green LED	LED indicates input power
DS2503	Red LED	LED indicates charging state

3.7.8 Debug Serial UART over USB J1600 (12)

The UART connection used on the Open-Q 845 is a USB micro B connector (J1600). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed. Use latest FTDI drivers from https://www.ftdichip.com/FTDrivers.htm instead of system update. See item 12 in Figure 1 for the location of J1600 on the carrier board.

3.7.9 USB 3.1 Type C (for ADB) J2300 (11)

The Open-Q 845 carrier board contains one USB 3.1 Type C connection (J2300). This connection is used for Android debug bridge (ADB) functionality. To get the adb shell, ensure that the board is up and running and connect the Type C cable between the board and the PC. Type the command adb root and adb shell on the PC prompt to exercise the adb shell functionality. While ADB utilizes only the high-speed channel, this USB type C connector supports the USB 3.1 specification including the super speed data channel. This USB connection is also uses as the charge source when the dev kit is powered by a battery and battery charging is enabled (see section 3.7.3 above). See item 11 in Figure 1 for the location of J2300 on the carrier board.

3.7.10 USB 3.1 Type A Connector J2400 (5)

The Open-Q 845 carrier board contains one USB Type A connector J2400 situated on the north side of carrier board, which exposes USB 3.1 host functionality. This USB connection is designed to provide up

to 1A VBUS current for external devices. See item 5 in Figure 1 for the location of J2400 on the carrier board.

If the user intend to use a mini-PCIe card on the dev kit that requires a USB connection (see 3.7.15 below), then the Mini-PCIe USB enable DIP switch S2401 (6) must be switched to closed / ON (figure below). If the DIP switch is closed, the USB 3.1 Type A connector is not functional.

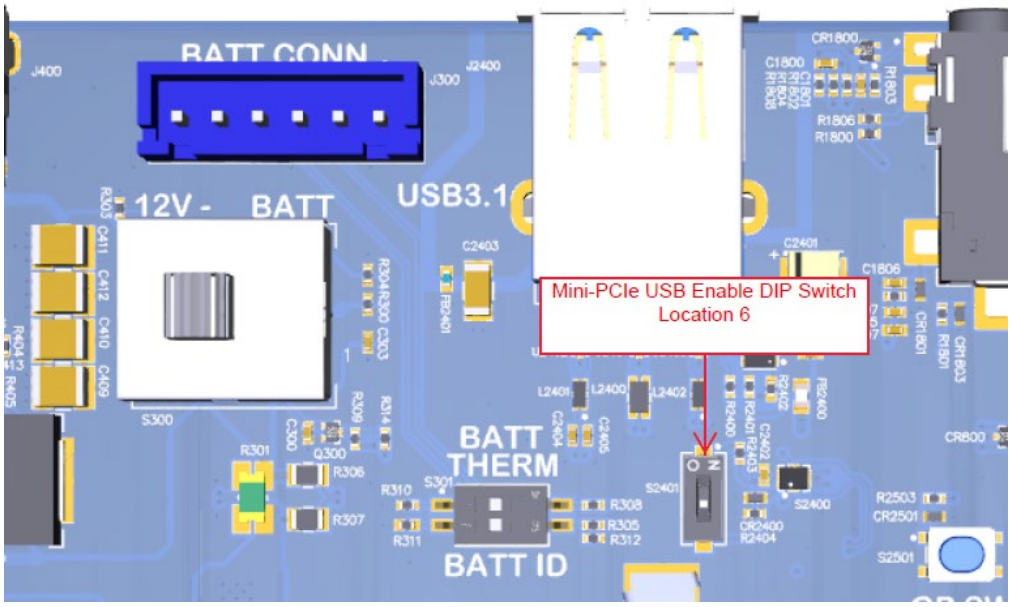

Figure 6. Mini-PCIe USB Enable DIP Switch (6)

3.7.11 Micro SD Card Socket J1500 (22)

J1500 (Micro-SD card connector) provides 4-bit secure digital (SD) interface for external storage. It is located on the bottom side of the carrier board right under the Display Module (see figure below). The SD interface supports High Speed mode.

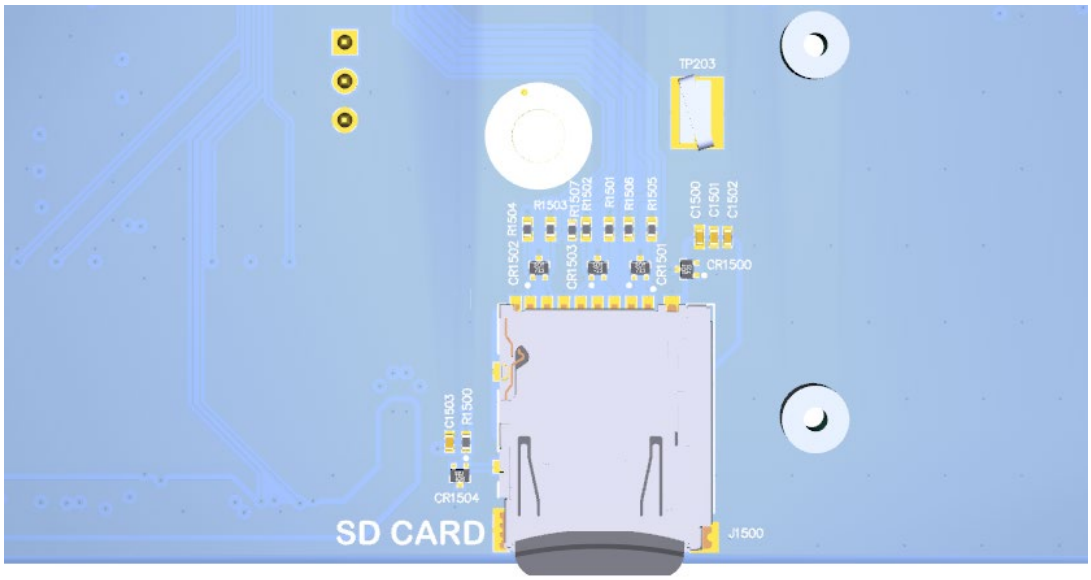

Figure 7. Micro SD Card Socket J1500

3.7.12 Display Connector J1400 (38)

The 100-pin display connector, J1400, allows for an optional display adapter to be connected to the development kit. Lantronix offers a compatible LCD panel accessory for the Open-Q 845 µSOM Development Kit. It can be purchased by contacting Lantronix Sales.

Exposed on the display connector are the following interfaces:

- Two 4-lane MIPI DSI high speed display interfaces
- LCD backlight control signals
- I2C bus for touch panel support
- Additional GPIOs for general purposes available
- Various power rails for powering the display adapter

For details on the signal list provided on the display connector, see the development kit schematic (R-3) and the display adapter design guide technical note document (R-4).

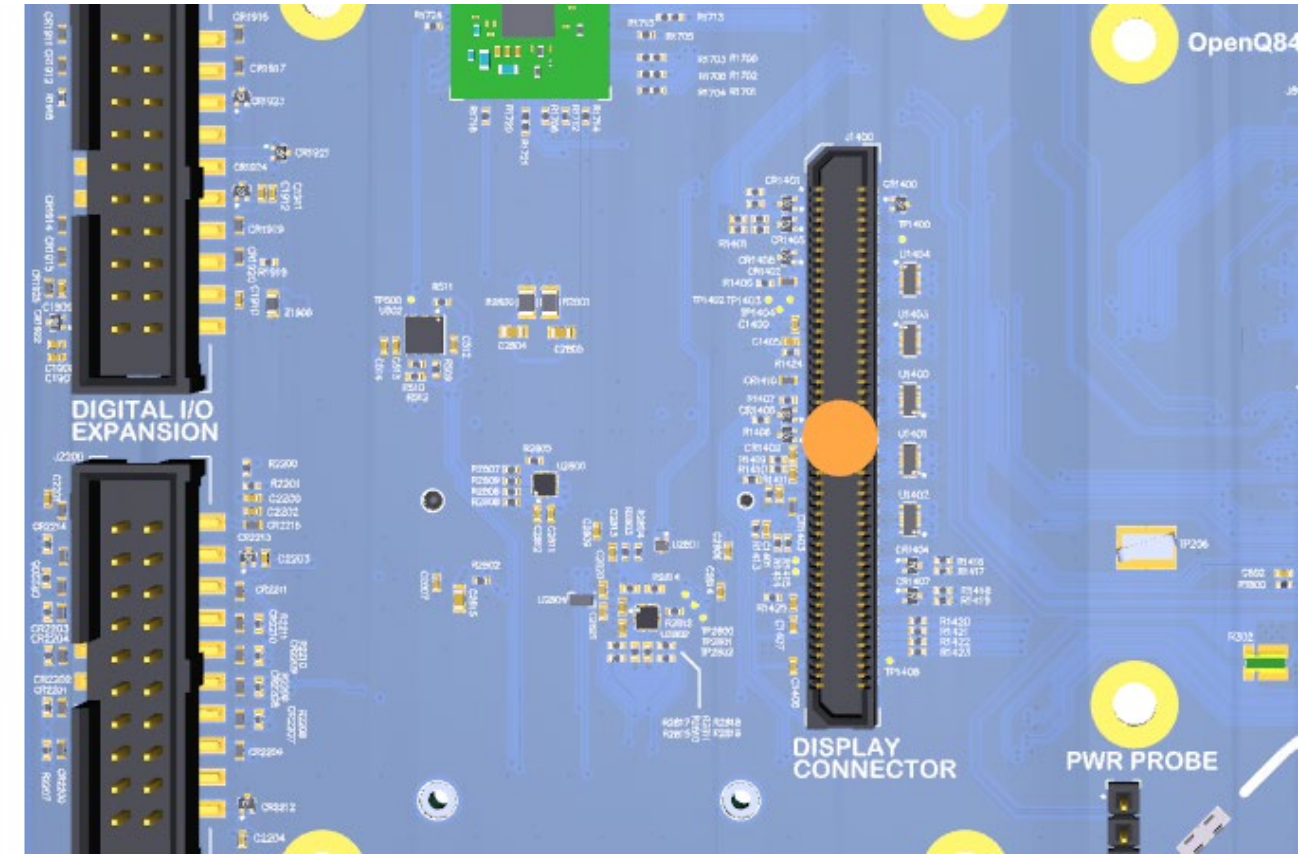

Figure 8. Display Connector J1400

3.7.13 Camera Connectors J1000 (15), J1100 (16), J1200 (17), J1300 (18)

The Open-Q 845 µSOM Development Kit includes four camera interface connectors, J1000, J1100, J1200, and J1300 allowing users to connect multiple camera adapters to the development kit. See items 15 through 18 in Figure 1 for the carrier board locations of the camera connectors.

Lantronix offers compatible camera module accessories for the Open-Q 845 µSOM Development Kit here: https://shop.intrinsyc.com/collections/accessories

Exposed on each camera connector are the following interfaces:

- One 4-lane MIPI CSI high speed camera interface
    - NOTE: The camera 4 connector J1300 includes only a 2-lane MIPI CSI interface.
- Camera Control Interface (CCI) I2C bus for camera and actuator control
- Additional GPIOs for general purposes available
- Various power rails for powering the camera adapter

For details on the signal list provided on the camera connectors, see the development kit schematic (R-3) and the camera adapter design guide technical note document (R-5).

3.7.14 Camera Flash Connectors J1001 (19) and J1201 (20)

In addition to the four camera connectors, the video capturing subsystem of the Open-Q 845 µSOM Development Kit is equipped with two connectors for flash or torch devices (J1001 and J1201). The PMI8998 power management IC has three flash channels, each with a maximum 1.5A rated regulated current sink. However, the development kit exposes only two of the flash channels with a 0.25A current limit, due to the current limit of the µSOM connectors pins.

See items 19 and 20 in Figure 1 for the carrier board locations of the camera flash connectors. The pinout of the connectors in shown in the table below. The typical interfacing to these camera flash channels is shown in the figure below.

Table 10. Camera Flash Connectors pinout

Pin No	Signal Name	Description
1	SOM_SYS_PWR_PER	System power 3.9V. Current limited to <0.5A
2	GND	System ground
3	GPIO_22_FL_STROBE_TRIG	CPU GPIO 22, input from external CMOS level flash trigger
4	FLASH_LED1 or FLASH_LED2	PMI8998 flash current sink channel 1 and 2, Full scale 0.24A regulated in 48 steps

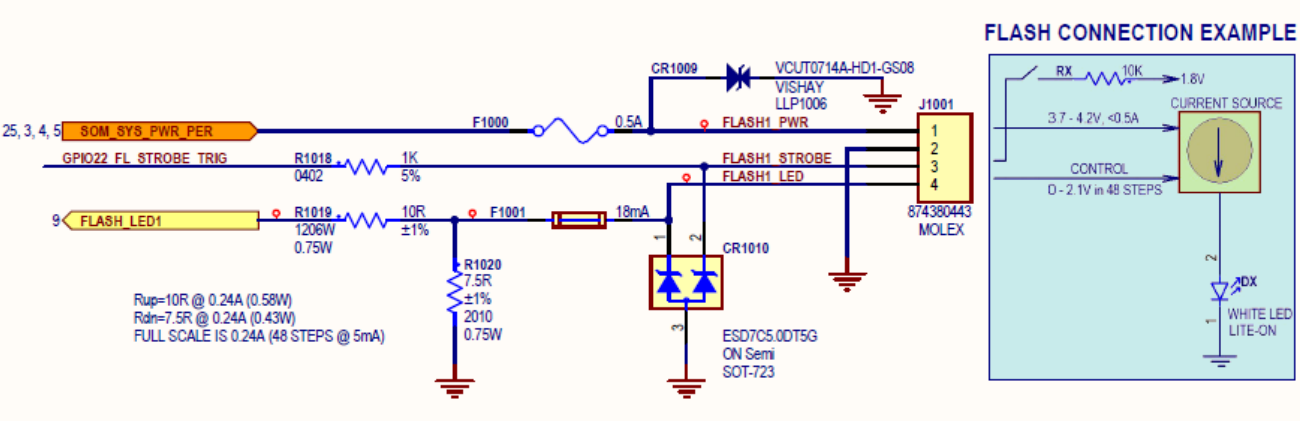

Figure 9. Typical Connection for Camera Flash Connector

3.7.15 Mini-PCIe Card Connector J2801 (24)

The Open-Q 845 µSOM Development Kit includes a mini-PCIe card socket J2801 (24) and an optional SIM card socket J2800 (25) on the bottom side of the carrier board (see image below).

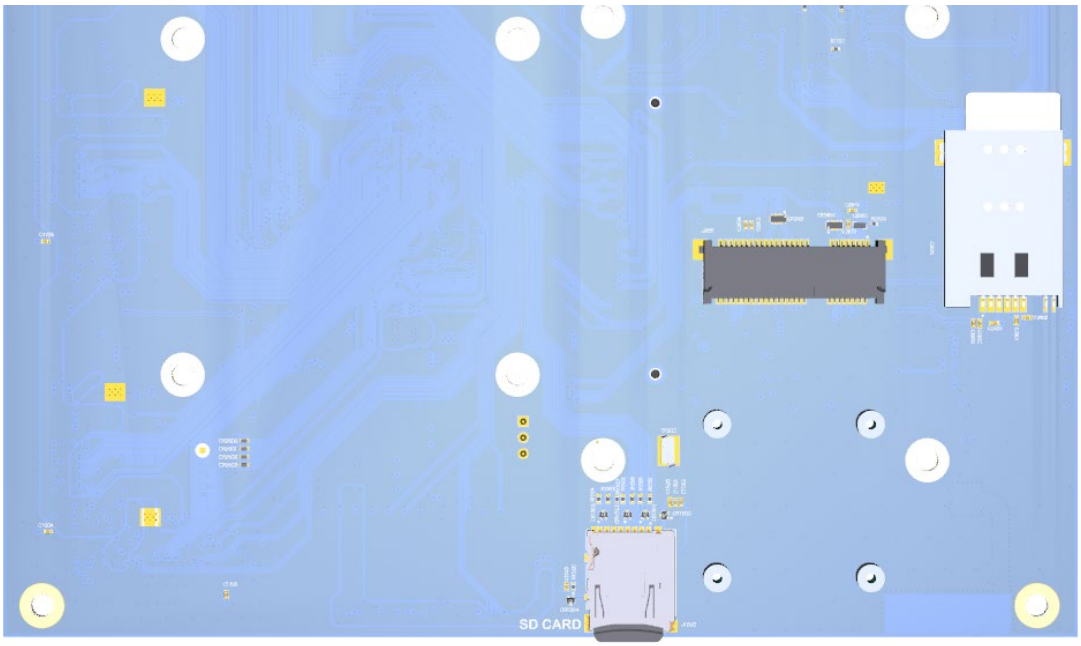

Figure 10. Mini-PCIe and Optional SIM Card Sockets

The Mini-PCIe card socket supports both the standard full and half size PCI Express mini cards with the 4 mounting holes located below J2800 in the image above. The pinout of J2800 complies with the PCI Express mini card standards. Please refer to the document at the following link for more information: https://www.pcisig.com/specifications/pciexpress/base/#mini1.2

The optional SIM card socket J2800 (25) can be used if the user is connecting a mini-PCIe card with cellular connection capabilities.

If the user intends to use a mini-PCIe card on the dev kit that requires a USB connection, then the Mini-PCIe USB enable DIP switch S2401 (6) must be switched to closed / ON. See Figure 6. Mini-PCIe USB Enable DIP Switch (6). If the DIP switch is closed, the USB 3.1 Type A connector J2400 (5) is not functional.

3.7.16 Digital IO Expansion Header J2200 (23)

The Open-Q 845 µSOM Development Kit includes a digital IO expansion header J2200 which provides access to a selection of µSOM GPIO signals and power rails. See item 23 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 11. Digital IO Expansion Header J2200 Pinout

Pin No	Signal	Description	Pin No	Signal	Description
1	VREG_S4A_1P8	µSOM LDO Regulator S4A +1.8V	2	VREG_S4A_1P8	µSOM LDO Regulator S4A +1.8V
3	SSC8_QUP2_0_SPI2_MISO	CPU Sensor Core SSC_GPIO8	4	MB_VREG_3P3	Carrier board switching regulator. 3.3V
5	SSC9_QUP2_1_SPI2_MOSI	CPU Sensor Core SSC_GPIO9	6	GPIO11_LCD_TE1	CPU GPIO11
7	SSC10_QUP2_2_SPI2_CLK	CPU Sensor Core SSC_GPIO10	8	GPIO0_QUP0_L0_SPI_MISO	CPU GPIO0
9	SSC11_QUP2_3_SPI2_CS_N	CPU Sensor Core SSC_GPIO11	10	GPIO1_QUP0_L1_SPI_MOSI	CPU GPIO1
11	GND	Ground	12	GPIO2_QUP0_L2_SPI_CLK	CPU GPIO2
13	GPIO56_QUP10_1_I2C_SCL	CPU GPIO56	14	GPIO3_QUP0_L3_SPI_CS_N	CPU GPIO3
15	GPIO55_QUP10_0_I2C_SDA	CPU GPIO55	16	GPIO7_LCD1_RST_N	CPU GPIO7
17	GND	Ground	18	GND	Ground
19	No Net		20	MB_VREG_5P0	Carrier board switching regulator +5.0V

For more details regarding configuring the GPIOs on this header, refer to the Open-Q 845 Software Release Notes to determine feature support in the latest software release.

3.7.17 Sensor IO Expansion Header J2100 (21)

The Open-Q 845 µSOM Development Kit includes a sensor expansion header J2100 which provides a connection to an optional sensor board. If sensor functionality is not required, this header may be used for other applications. See item 21 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 12 - Sensor Expansion Header J2100 Pinout

Pin No	Signal	Description	Pin No	Signal	Description
1	SSC0_QUP0_0_I2C1_SDA	CPU Sensor Core SSC_GPIO0	2	GPIO117_ACCEL_INT	CPU GPIO117
3	SSC1_QUP0_1_I2C1_SCL	CPU Sensor Core SSC_GPIO1	4	GPIO123	CPU GPIO123
5	GPIO63_QUA_MI2S_DATA3	CPU GPIO63	6	GPIO118_GYRO_INT	CPU GPIO118

7	VREG_LVS2A_1P8	µSOM low voltage switch LVS2 +1.8V	8	VREG_L19A_3P0	µSOM LDO L19A +3.0V
9	GND	Ground	10	GND	Ground
11	GPIO122_HRM_INT	CPU GPIO122	12	GPIO125_TS_INT_N	CPU GPIO125
13	SSC6_QUP1_4_SPI1_CS1_N	CPU Sensor Core SSC_GPIO6	14	GPIO120_ALSP_INT_N	CPU GPIO120
15	GPIO62_QUA_MI2S_DATA2	CPU GPIO62	16	GPIO119_MAG_INT_N	CPU GPIO119
17	No Net		18	GPIO124	CPU GPIO124
19	SSC5_QUP1_3_SPI1_CS0_N	CPU Sensor Core SSC_GPIO5	20	SSC3_QUP1_1_SPI1_MOSI	CPU Sensor Core SSC_GPIO3
21	SSC4_QUP1_2_SPI1_CLK	CPU Sensor Core SSC_GPIO4	22	SSC2_QUP1_0_SPI1_MISO	CPU Sensor Core SSC_GPIO2
23	No Net		24	SSC7_QUP1_5_SPI1_CS2_N	CPU Sensor Core SSC_GPIO7

For more details regarding configuring the GPIOs on this header, refer to the Open-Q 845 Software Release Notes to determine feature support in the latest software release.

3.7.18 Audio Inputs Expansion Header J1900 (27)

The Open-Q 845 µSOM Development Kit audio subsystem is built around the Qualcomm Audio Codec WCD9340 (28). The Audio Inputs Expansion Header J1900 exposes some of the audio input capabilities of WCD9340 for the user. See item 27 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 13. Audio Inputs Expansion Header Pinout J1900

Pin No	Signal	Description	Pin No	Signal	Description
1	CDC_IN1_P	Codec Input 1 Positive	2	CDC_IN1_N	Codec Input 1 Negative
3	CDC_IN3_P	Codec Input 3 Positive	4	CDC_IN3_N	Codec Input 3 Negative
5	CDC_MIC_BIAS1	Microphone Bias 1	6	CDC_MIC_BIAS3	Microphone Bias 3
7	CDC_IN4_P	Codec Input 4 Positive	8	CDC_IN4_N	Codec Input 4 Negative
9	CDC_MIC_BIAS4	Microphone Bias 4	10	MB_VREG_3P3	Carrier board switching regulator +3.3V
11	GND	System Ground	12	GND	System Ground
13	CDC_DMIC_CLK0	Digital Microphone 0 Clock	14	CDC_DMIC_CLK1	Digital Microphone 1 Clock
15	CDC_DMIC_DATA0	Digital Microphone 0 Data	16	CDC_DMIC_DATA1	Digital Microphone 1 Data
17	VREG_S4A_1P8	µSOM LDO Regulator S4A +1.8V	18	CDC_DMIC_CLK2	Digital Microphone 2 Clock
19	GND	System Ground	20	CDC_DMIC_DATA2	Digital Microphone 2 Data

3.7.19 Audio Outputs Expansion Header J1901 (26)

The Open-Q 845 µSOM Development Kit audio subsystem is built around the Qualcomm Audio Codec WCD9340 (28). The Audio Outputs Expansion Header J1901 exposes some of the audio output capabilities of WCD9340 for the user. See item 26 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 14. Audio Outputs Expansion Header Pinout J1901

Pin No	Signal	Description	Pin No	Signal	Description
1	CDC_LINE_OUT1_P	Codec Line Out 1 Positive	2	CDC_LINE_OUT1_N	Codec Line Out 1 Negative
3	CDC_LINE_OUT2_P	Codec Line Out 2 Positive	4	CDC_LINE_OUT2_N	Codec Line Out 2 Negative
5	CDC_LINE_REF	Codec Reference (GND)	6	MB_VREG_3P3	Carrier board switching regulator +3.3V
7	GND	System Ground	8	GND	System Ground
9	CDC_EAR_P	Earphone Amplifier Output Positive	10	CDC_EAR_N	Earphone Amplifier Output Negative
11	GND	System Ground	12	SOM_SYS_PWR_PER	SOM System Power
13	CDC_SWR_CLK	Codec PDM Clock	14	CDC_SWR_DATA	Codec PDM Data
15	CDC_WSA_EN	Codec GPIO, can be used as Speaker Amp Enable 1	16	PMI8998_SPKR_AMP_EN2	µSOM PMIC GPIO11, can be used as Speaker Amp Enable 2
17	VREG_S4A_1P8	µSOM LDO Regulator S4A +1.8V	18	DC_IN_12V	Voltage from DC Power Input +12.0V
19	MB_VREG_5P0	Carrier board switching regulator +5.0V	20	GND	System Ground

For more details regarding configuring the GPIOs on this header, refer to the Open-Q 845 Software Release Notes to determine feature support in the latest software release.

3.7.20 Audio IO Expansion Header J2000 (10)

In addition to the Qualcomm Audio Codec WCD9340 (28), the Open-Q 845 µSOM Development Kit also includes other digital audio interfaces. The Audio IO Expansion Header J2000 exposes some of these interfaces for the user. See item 10 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 15. Audio IO Expansion Header Pinout J2000

Pin No	Signal	Description	Pin No	Signal	Description
1	GPIO57_FORCE_USB_BOOT	CPU GPIO57 – can be configured as QUA_MI2S_MCLK	2	GND	Ground

Pin No	Signal	Description	Pin No	Signal	Description
3	GPIO58_QUA_MI2S_SCK	CPU GPIO58 – can be configured as QUA_MI2S_SCK	4	GPIO61_QUA_MI2S_DATA1	CPU GPIO61 – can be configured as QUA_MI2S_DATA1
5	GPIO59_QUA_MI2S_WS	CPU GPIO59 – can be configured as QUA_MI2S_WS	6	GPIO62_QUA_MI2S_DATA2	CPU GPIO62 – can be configured as QUA_MI2S_DATA2
7	GPIO60_QUA_MI2S_DATA0	CPU GPIO60 – can be configured as QUA_MI2S_DATA0	8	GPIO63_QUA_MI2S_DATA3	CPU GPIO63 – can be configured as QUA_MI2S_DATA3
9	GND	Ground	10	GPIO64_CODEC_RST_N	CPU GPIO64 – can be configured as PRI_MI2S_MCLK (see Note 1 below)
11	GPIO65_CODEC_SPI_MISO	CPU GPIO65 – can be configured as PRI_MI2S_SCK (see Note 1 below)	12	GND	Ground
13	GPIO66_CODEC_SPI_MOSI	CPU GPIO66 – can be configured as PRI_MI2S_WS (see Note 1 below)	14	LN_BB_CLK2_WCD_CON	µSOM PMIC baseband clock output (see Note 1 below)
15	GPIO67_CODEC_SPI_CLK	CPU GPIO67 – can be configured as PRI_MI2S_DATA0 (see Note 1 below)	16	No net	
17	GPIO68_CODEC_SPI_CS_N	CPU GPIO68 – can be configured as PRI_MI2S_DATA1 (see Note 1 below)	18	CDC_IN5_P	Codec Input 5 Positive
19	GND	Ground	20	CDC_IN5_N	Codec Input 5 Negative
21	GPIO69_SPKR_I2S_SCK	CPU GPIO69 – can be configured as SPKR_I2S_SCK	22	GND	Ground
23	GPIO70_CODEC_SLIMBUS_CLK_CON	CPU GPIO70 – can be configured as SPKR_I2S_CLK (see Note 1 below)	24	No net	
25	GPIO71_CODEC_SLIMBUS_DATA0_CON	CPU GPIO71 – can be configured as SPKR_I2S_DATA_OUT (see Note 1 below)	26	CDC_MIC_BIAS1	Microphone Bias 1
27	GPIO72_CODEC_SLIMBUS_DATA1_CON	CPU GPIO72 – can be configured as SPKR_I2S_WS (see Note 1 below)	28	CDC_LDO_H	WCD9340 Audio Codec LDO output
29	GND	Ground	30	No net	
31	MB_VREG_1P8	Carrier board switching regulator +1.8V	32	GND	Ground
33	MB_VREG_3P3	Carrier board switching regulator +3.3V	34	GPIO54_CODEC_INT1_CON	CPU GPIO54 (see Note 1 below)
35	MB_VREG_5P0	Carrier board switching regulator +5.0V	36	GPIO53_CODEC_INT2_CON	CPU GPIO53 (see Note 1 below)

Pin No	Signal	Description	Pin No	Signal	Description
37	DC_IN_12V	Voltage from DC Power Input +12.0V	38	No net	
39	GND	Ground	40	MB_VREG_1P8	Carrier board switching regulator +1.8V

1. Population option changes are necessary in order to use this signal. See the carrier board schematic (R-3) for more details.

For more details regarding configuring the GPIOs on this header, refer to the Open-Q 845 Software Release Notes to determine feature support in the latest software release.

3.7.21 Audio Headset Jack J1800 (8)

In addition to the audio expansion headers, the Open-Q 845 µSOM Development Kit also includes a standard 3.5mm audio headset jack J1800, which provides connection to headphone, microphone input and headset detection circuits. See item 8 in Figure 1 for the carrier board location of this headset jack.

3.7.22 WLAN / BT Antenna Connections (13, 14)

The Open-Q 845 µSOM Development Kit WLAN/BT functionality is based on Qualcomm WCN3990 chipset. It provides WLAN/Bluetooth in 2x2 MIMO with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards, and Bluetooth + LE 5.x + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.

The WCN3990 chipset is located on the µSOM, which has U.FL coax connectors for channel 0 (WLAN+BT) and channel 1 (WLAN only). These connectors are mated to the Carrier board WLAN / BT PCB antennas via coax cables. Figure 1 in 3.4.1 above shows how the two WLAN / BT are routed via the coax cables:

- For channel 0 (WLAN+BT), see items 31 and 13 on Figure 1.
- For channel 1 (WLAN only), see items 32 and 14 on Figure 1.

If a more advanced antenna solution is required, it is possible to connect custom antennas directly to the µSOM U.FL connectors.

3.7.23 Quiet Thermistor RT800 (35)

The Open-Q 845 µSOM Development Kit includes a thermistor on the carrier board to allow for system level thermal management. See item 35 in Figure 1 for the carrier board location of the Quiet Thermistor RT800.

3.7.24 Haptic Output Header J802 (9)

The Open-Q 845 µSOM Development Kit includes a haptic output header J802, giving the user access to the µSOM PMI8998 PMIC haptic output driver. This driver supports both ERM and LRA modes. See item 9 in Figure 1 for the carrier board location of this header. The pinout for this header is shown in the table below.

Table 16. Haptic Output Header Pinout J802

Pin No	Signal	Description
1	HAP_OUT_R_P	Haptic output positive
2	HAP_OUT_R_N	Haptic output negative