LANTRONIX® Formerly INTRINSYC

Open-Q™ 410 Development Kit User Guide

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Contacts

Lantronix, Inc.
7535 Irvine Center Drive, Suite 100
Irvine, CA 92618, USA
Toll Free: 800-526-8766
Phone: 949-453-3990
Fax: 949-453-3995

IES Customer Support Portal
https://helpdesk.intrinsyc.com

Lantronix Technical Support
http://www.lantronix.com/support

Sales Offices
For a current list of our domestic and international sales offices, go to the Lantronix web site at http://www.lantronix.com/about-us/contact/

Revision History

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July 2015	1.1	Updates after review
August 2015	1.2	Updated section 4.7, S501 to OFF
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August 2020	A	Initial Lantronix document. Added Lantronix document part number, Lantronix logo, branding, contact information, and links.

For the latest revision of this product document, please go to: http://tech.intrinsyc.com.

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1 Introduction

This user guide includes information needed for users to become familiar with the Open-Q™ 410 Development Kit based on the Qualcomm® APQ8016E processor. The document includes:

- Block Diagrams
- Configuration Options
- System on Module (SOM) hardware features
- Carrier Board hardware features
- Optional Accessories

For background information on the kit, go to: https://www.lantronix.com/products/open-q-410-development-kit/

1.1 Intended Audience

This document is intended for end users who have purchased an Open-Q™ 410 Development Kit from the Lantronix web store:

http://shop.intrinsyc.com/collections/qualcomm

1.2 Applicable Documents

Reference	Title
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q™ 410 Development Kit

1.3 Reference Documents

Reference	Title
R-1	Open- Q™ 410 Development Kit Display Board Design Guide Tech Note
R-2	Open- Q™ 410 Development Kit Camera Board Design Guide Tech Note
R-3	Open- Q™ 410 Development Kit Carrier Board Design Guide Tech Note
R-4	Open- Q™ 410 SOM Development Kit HW Revision Guide

1.4 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral; (Serial interfaces like UART/SPI/I2C/UIM)
BT LE	Bluetooth Low Energy
CB	Carrier Board
CSI	Camera Serial Interface
DP	Display Port
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read Only Memory
eMMC	embedded Multi-Media Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning System
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry Processor Interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SMARC	Smart Mobility ARChitecture Specification - Published by Standardization Group for Embedded Technologies
SOM	System-On-Module
SPMI	System Power Management Interface (QUALCOMM PMIC / baseband proprietary protocol)

Term and acronyms	Definition
UART	Universal Asynchronous Receiver Transmitter
UIM	User Identity Module
USB	Universal Serial Bus
USB HS	USB High-Speed
USB SS	USB Super-Speed

2 Overview

The Open-Q™ 410 Development Kit provides an evaluation platform for Qualcomm™ APQ8016E processor. This kit is ideally suited for Android / Linux / Windows Application developers, OEMs, Consumer manufacturers, Hardware Component Vendors, Video Surveillance, Robotics, etc. to evaluate, optimize, test and deploy applications that can utilize the Qualcomm APQ8016E series technology.

2.1 Development Device Notice

This development device contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is intended for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development device is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development device may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at:

http://www.fcc.gov/oet/rfsafety/

2.2 Anti-Static Handling Procedures

The Open-Q™ 410 Development Kit is an open frame PCB assembly with exposed integrated circuits. Accordingly, proper anti-static precautions should be employed when handling the kit, including:

- Use a grounded anti-static mat
- Use a grounded wrist or foot strap

2.3 Kit Contents

The Open-Q™ 410 Development Kit is shipped with the following (see figure below):

- Open-Q™ 410 SOM with APQ8016E processor
- Android 5.0 (lollipop) pre-loaded
- 13mm x 13mm Carrier Board
- AC power adapter

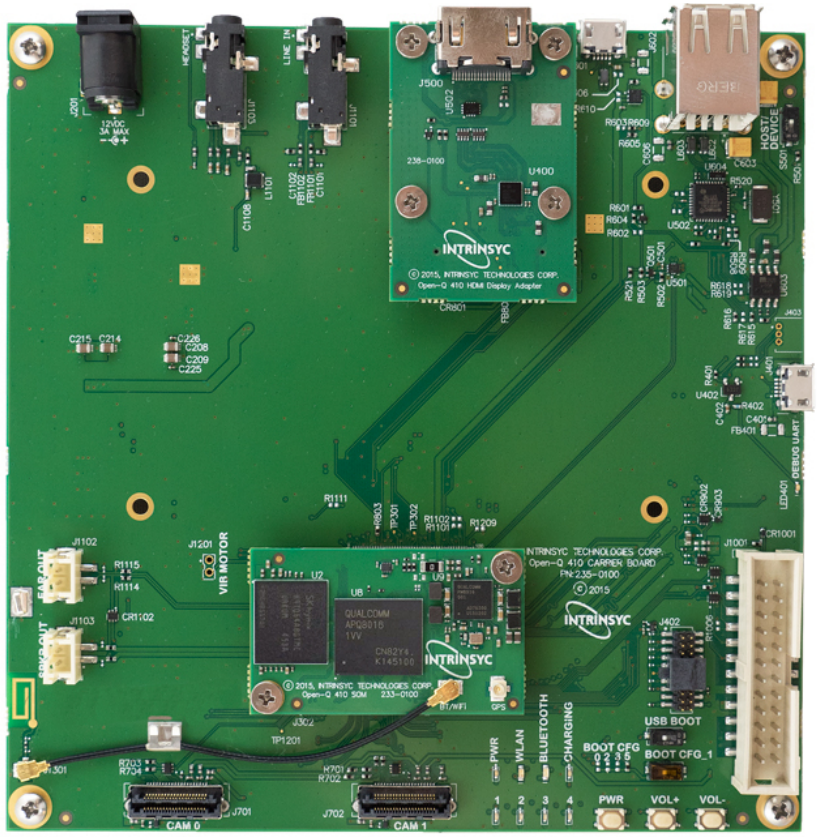

Figure 1 – Assembled Open-Q 410 Development Kit

There are also some optional accessories available for the Open-Q 410 Development Kit, such as:

- Open-Q™ 5MP (OmniVision OV5640) Camera Module (For Rev 0100)
- Open-Q™ 13MP (Sony IMX214) Camera Module (For Rev 0200)
- 4.46" FWVGA MIPI DSI LCD with capacitive multi-touch
- 4.5" FWVGA MIPI DSI LCD with capacitive multi-touch

For details on purchasing accessories, go to:

http://shop.intrinsyc.com/collections/dragonboard-accessories

2.4 Hardware Identification Labels

Labels are present on the SOM and Carrier boards that include the following information:

- SOM Serial Number
- SOM Wi-Fi MAC Address
- Carrier Board Serial Number

Users are required to enter their SOM serial number when registering on:

http://helpdesk.intrinsyc.com

NOTE:

Users should retain a copy of the SOM and Carrier Board label information for warranty and support purposes.

2.5 Block Diagram

The block diagram for the Open-Q™ 410 Development Kit is shown below.

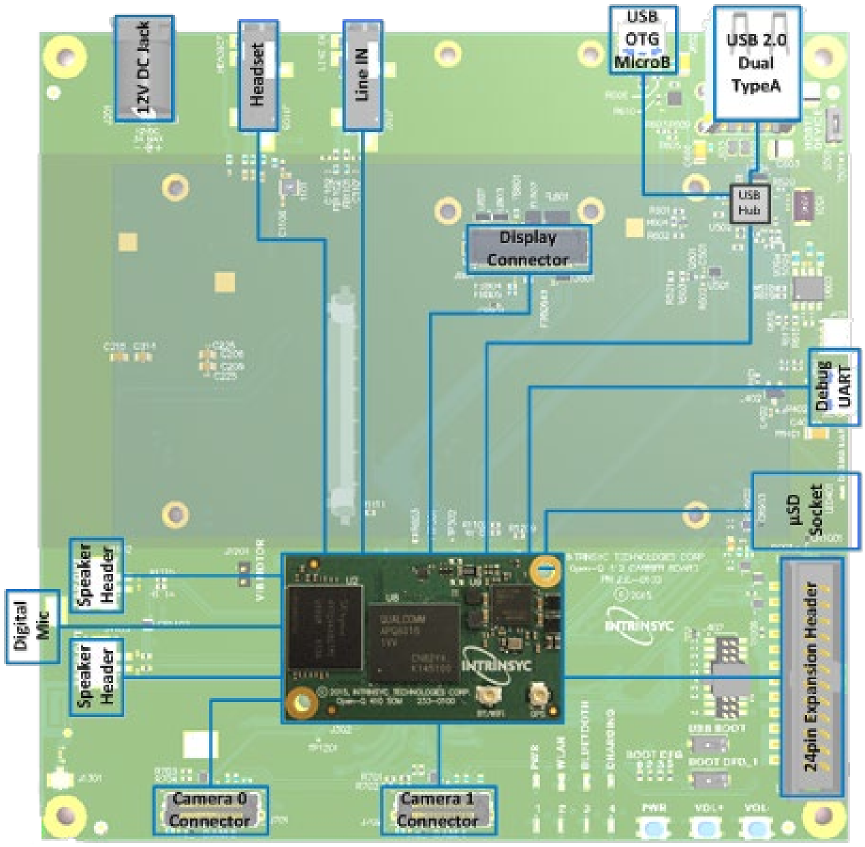

Figure 2 – Open-Q™ 410 Development Kit Block Diagram (Rev 0100 shown here)

2.6 Feature List

The table below lists the features of the Open-Q 410 Development Kit hardware.

Table 1 – Open-Q 410 Development Kit Hardware Features

Subsystem or Connectors	Feature Set	Description	Specification
Chipset	APQ8016E	Qualcomm™ APQ8016E	64-bit Quad 1.2GHz ARM Cortex-A53 with 512kB L2 cache. Adreno™ A306 3D graphics core.
	PM8916	QUALCOMM® companion PMIC for APQ8016E processor	Includes audio codec functionality

Subsystem or Connectors	Feature Set	Description	Specification
Memory	1GB LPDDR3	32-bit 533MHz	embedded multi chip package (eMCP)
	8 GB eMMC	eMMC4.5 / HS200	embedded multi chip package (eMCP)
Connectivity	Wi-Fi 2.4Ghz via WCN3620	QUALCOMM® WCN3620 Wi-Fi + BT Combo Chip	802.11b/g/n single band
	BT 4.0 via WCN3620	QUALCOMM® WCN3620 Wi-Fi + BT Combo Chip	BT 4.0 + BLE
	GPS receiver	QUALCOMM® WGR7640	GPS, GLONASS, COMPASS
RF Interfaces	1x WLAN / BT Antenna Connectors on SOM and 1 PCB Antennas on Carrier Board	Internal/External BT / WIFI Antenna	U.FL connector
	1x GPS Antenna Connectors on SOM	External GPS Antenna connector	U.FL connector
Audio	Headset support	Headset connection with stereo output, microphone input and jack detection	3.5mm Modular Jack
	Audio input	Stereo line input	3.5mm Modular Jack
	Audio output	Loud speaker and earpiece audio outputs	
	Digital Mic	Digital microphone input	
Buttons	Power Button	Power Button	NA
	Volume Up	Increase Volume Button	NA
	Volume Down	Decrease Volume button/ Reset	NA
Indicating LED	Power ON	Power presence indicator. Red LED	

Subsystem or Connectors	Feature Set	Description	Specification
	USER LED 1-4	User LEDs	
Sensors & IoT Expansion	Sensor / IoT Expansion Header	Support for Sensor (optional ST Micro sensor board) Support for Lantronix IoT Development Kit	
Interfaces and Connectors	1 x DC Jack	DC Power Supply	
	1 x Battery Development	Reserved to give customer possibility of battery input	
	1 x MIPI DSI	60 Pin Display Connector Optional MIPI based 4.5" Truly display	4-lane MIPI Alliance Specification v1.01
	2 x MIPI CSI	Camera Connectors	4-lane and 2-lane MIPI Alliance Specification v1.0 compliant
	1 x Micro SD card Slot	4-bit, Dual-Voltage (1.8/2.95 V) up to 200MHz Push-Push Micro SD Card Slot	Supports XDHC/ SDHC and SDIO v3.0
	1 x HDMI	optional HDMI output supported via HDMI adapter board.	HDMI 1.4a, Type A
	1 x USB2.0 device	Micro-B USB 2.0 Connector	
	2 x USB2.0 host	Dual Type-A USB 2.0 Connector	
	Debug UART	Debug UART via USB Micro-B connector	FTDI UART to USB Bridge
	1 x JTAG	JTAG header	

2.7 Custom Hardware Configurations

The Open-Q™ 410 Development Kit provides is a flexible platform for validating functionality of the ultra-small 26.5mm x 44mm Open-Q™ 410 SOM that is included with the kit. The small size of the SOM allows for it to be capable of being designed into a multitude of configurations and custom enclosures. Reference documents R-1 through R-3 describe how to design custom carrier boards and peripherals for specific applications. For information on how Lantronix can assist in the development of custom hardware and software designs, go to:

http://helpdesk.intrinsyc.com

3 Open-Q™ 410 SOM

The Open-Q™ 410 (APQ8016E) SOM measures 26.5mm x 44mm. A top view of the SOM is shown below.

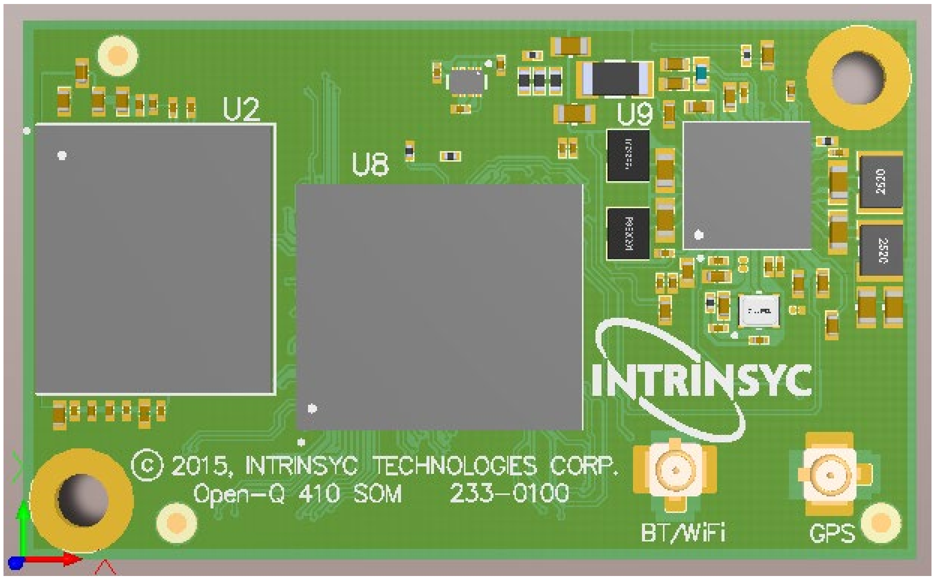

Figure 3 – Top View of Open-Q 410 SOM

The SOM connects to the Carrier Board with two 100-pin board to board connectors, as shown by the bottom side view below.

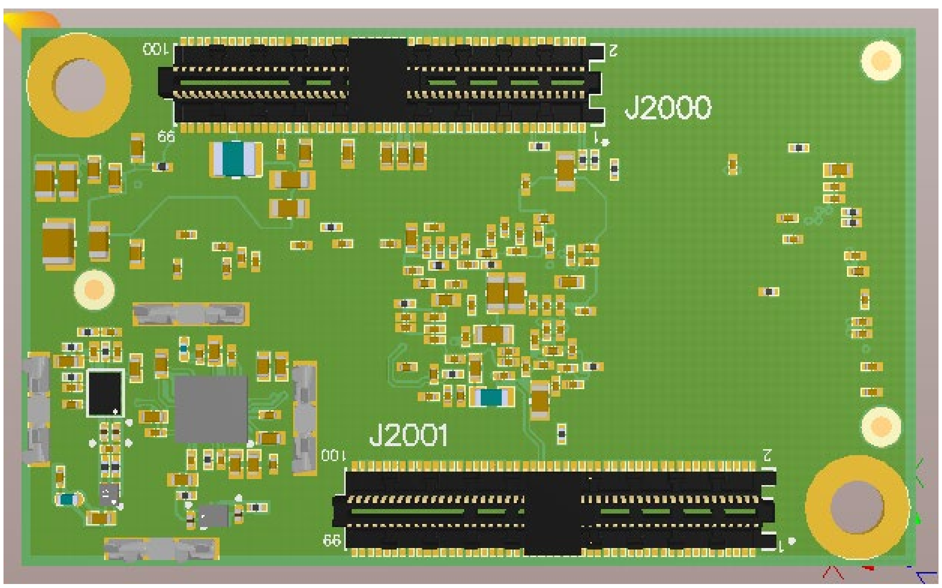

Figure 4 – Bottom View of Open-Q 410 SOM

The block diagram for the SOM is shown below.

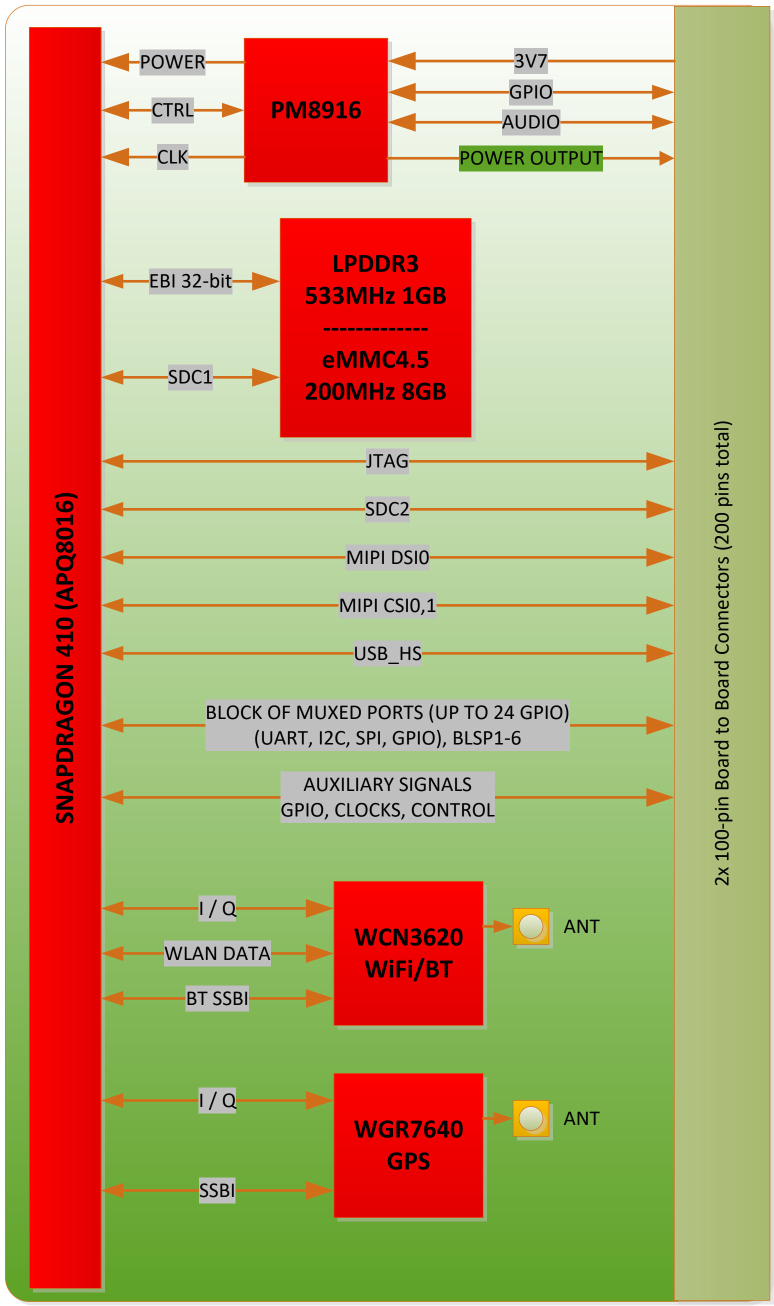

Figure 5 – Open-Q™ 410 (APQ8016E) SOM Block Diagram

The Open-Q™ 410 Development Kit is provided with the SOM connected and secured to the Carrier Board. The sections below include more information for the development kit user.

3.1 Carrier Board Connection

The SOM provides the basic common set of features with minimal integration efforts for end users. This is achieved with two 100-pin board to board connectors that interface the SOM to the carrier board. The connectors used are the Samtec ST4 / SS4 family providing a 4mm stack height between the SOM and carrier board. There are also two mounting holes that allow for an M2.5 screw assembly to be used for securing the two boards together.

3.2 Wi-Fi / BT Antenna Connection

The SOM includes a U.FL coaxial connector on the top side, which provides the connection to the single band Wi-Fi / BT antenna feed from the WCN3620. The Open-Q 410 Development Kit is shipped with this antenna feed connected to a PCB trace antenna on the Carrier board with a U.FL coaxial cable.

The SOM has received Wi-Fi modular regulatory certifications (see FCC ID: 2AFDI-ITCOQ410S for details). Please note that the on-board PCB antenna is not the antenna used for the SOM Wi-Fi/BT module certification.

3.3 GPS Antenna Connection

The SOM includes a U.FL coaxial connector on the top side, which provides the connection to the GPS antenna feed from the WGR7640. The user can gain access to GPS location data by connecting an external active antenna to the GPS connector on the SOM. The GPS connector can only supply 1.8V DC, so an external active antenna that can operate at 1.8V DC is required. A possible GPS antenna to use is the Taoglas AP.17F.07.0064A. **A passive antenna can be used only if the antenna is DC-open**. A passive antenna that has a DC-short will disable GPS function or damage the system. For reference, system is tested with a passive antenna (Taoglas FXP611.07.0092C) to assure functionality

4 Open-Q™ 410 Carrier Board

The Open-Q™ 410 (APQ8016E) Carrier Board measures 13mm x 13mm. See Figure 2 for the carrier board block diagram.

The sections below provide more information on the Carrier Board feature list listed in section 2. This information may be useful for development kit users who want to connect other devices or peripherals to the platform. If there are any discrepancies between this document and the development kit schematics, the latter shall take precedence.

4.1 Boot Configuration Options

The Open-Q™ 410 CPU boot mode is selected by two DIP switches found on the carrier board as shown in the figure below.

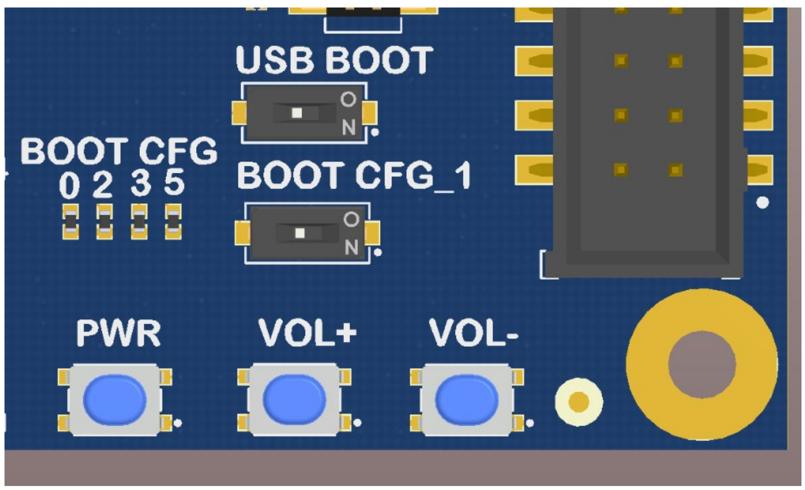

Figure 6 – Buttons, LEDs, and Boot Configuration

The user can select the boot mode of the CPU by setting the two DIP switches according to the following table.

Table 2 – Boot Configuration Options

BOOT OPTIONS	USB BOOT DIP Switch	BOOT CFG_1 DIP Switch	DEFAULT
USB force boot	ON	X	
1. SDC1 (eMMC on SOM) 2. SDC2 (µSDµ socket on Carrier) 3. USB2.0	OFF	OFF	Default configuration
1. SDC2 (µSDµSD socket on Carrier) 2. SDC1 (eMMC on SOM) 3. USB2.0	OFF	ON	

4.2 Buttons and LEDs

There are three buttons on the Carrier Board: Power On/Off, Volume Up and Volume Down. There are also eight LEDs: Power indicator, User LEDs #1 – 4, WLAN activity, BT activity, and charging status. The positions of the buttons and LEDs are shown in the figure above.

4.3 Power and Battery Connections

The main power input barrel connector (J201) is located on the top side of Carrier Board, as shown below.

The main power input requires a 10-16VDC supply rated for at least 3A. Lantronix encourages using the 12VDC / 3A power supply provided with the kit. The main power input is protected by a very fast acting 5A rated fuse. J201 is a center pin positive, 2.5mm barrel jack.

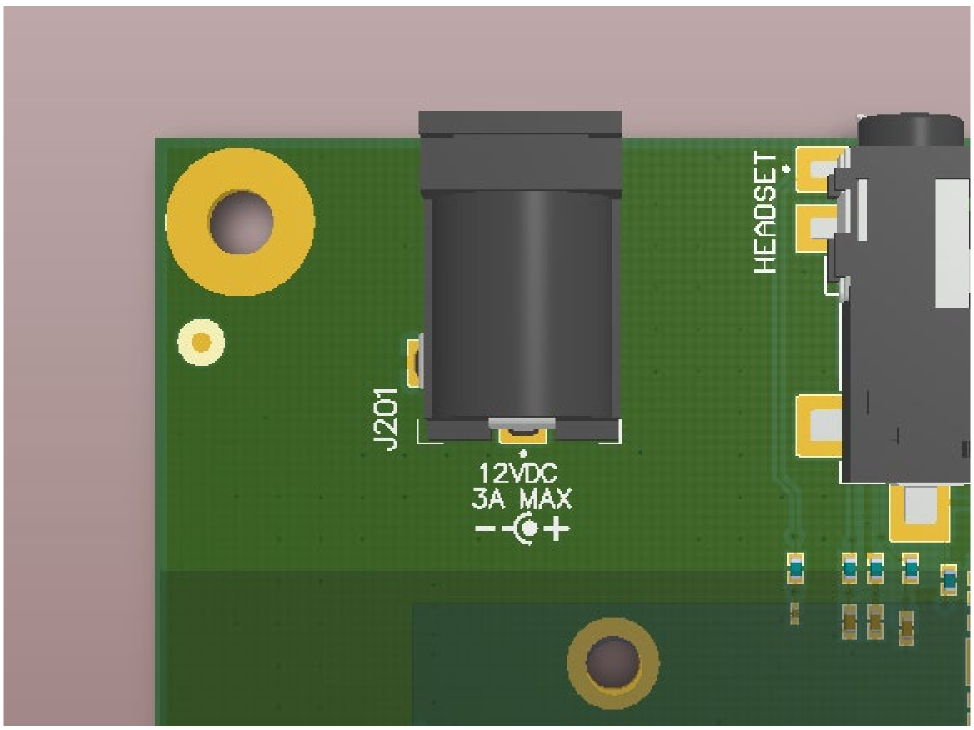

Figure 7 – Power Input Jack

There also exists a 6-pin battery input header on the bottom side of the PCB at J1202, as shown below. If the user would like to use this header, the following must be done:

- Remove resistors R207 and R209. This will disable the on-board 3.7V buck power supply and allow the battery header to drive this power rail to the SOM.
- Connect a single cell Lithium battery to J1202 (see pinout details below).
- Remove R1214 in order to enable the linear battery charger on the SOM.
- See figure below for respective resistors and connector location

IMPORTANT NOTES:

1. If the battery input header is used as above, the external +12V DC power supply must still be connected on the carrier board in order to keep the on-board +5V buck power supply operational.

2. See software release notes for the latest status of battery support in the 410 BSP. Otherwise, contact Lantronix for assistance in enabling battery operation in your BSP.

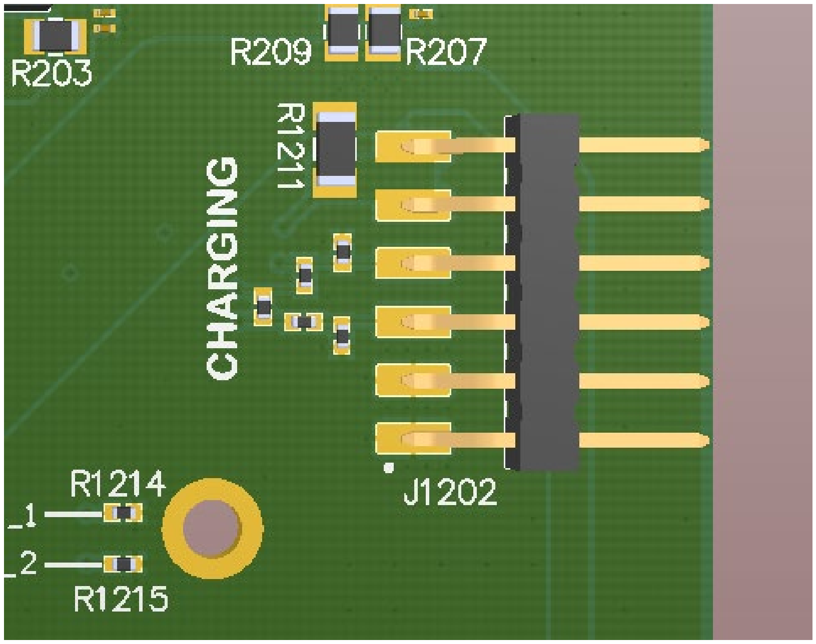

Figure 8 – Battery Input Header

The pinout for the J1202 battery header is shown in the table below.

Table 3 – Battery Input Header Pinout

Pin#	Signal Name (J1202)	Description
1, 2	GND	Ground
3	BATT_THERM_CONN	Battery pack thermistor connection
4	BATT_ID	Battery pack ID connection
5, 6	VBATT_CONN_SENSE	Single cell battery pack positive connection (3.7V typical)

4.4 Debug Serial UART over USB

The Open-Q™ 410 Development Kit includes a debug serial UART connection over a micro-B USB connector (J401), as shown below. The UART over USB connection is implemented using the FTDI FT234XD chip on the carrier board. The user can have a functional serial terminal working on a PC by ensuring that the appropriate

FTDI drivers are installed. User can also bypass the FTDI chip and have direct access to the UART TTL signal by removing R417, R418 and installing R420, R421, and J403 (not installed by default) on the carrier board.

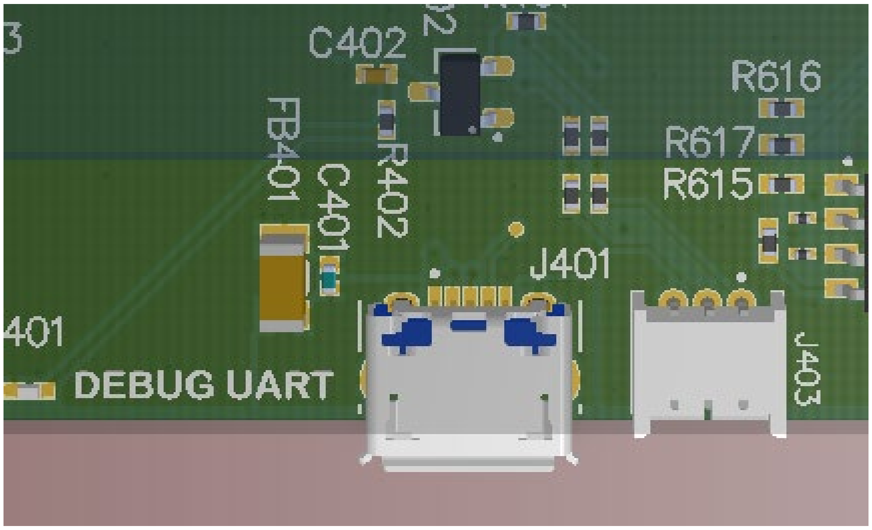

Figure 9 – Debug Serial UART over USB (J401)

4.5 MIPI CSI Camera Connectors

There are two different versions of the Open-Q™ 410 carrier board.

- Rev 0100 uses the Samtec LSHM series connector (model #: LSHM-120-02.5-L-DV-A-S-K-TR) to connects to the Open-Q™ 5MP (OmniVision OV5640) Camera Module
- Rev 0200 uses the JAE FI-R series connector (Model #: FI-RE41S-VF) connector to connects to the Open-Q™ 13MP (Sony IMX214) Camera Module

4.5.1 Open-Q™ Carrier Board Rev 0100

The Rev 0100 Open-Q™ 410 carrier board has two MIPI CSI camera connectors: J701 and J702. The two Samtec LSHM-120-02.5-L-DV-A-S-K-TR 40-pins connector are shown in the figure below.

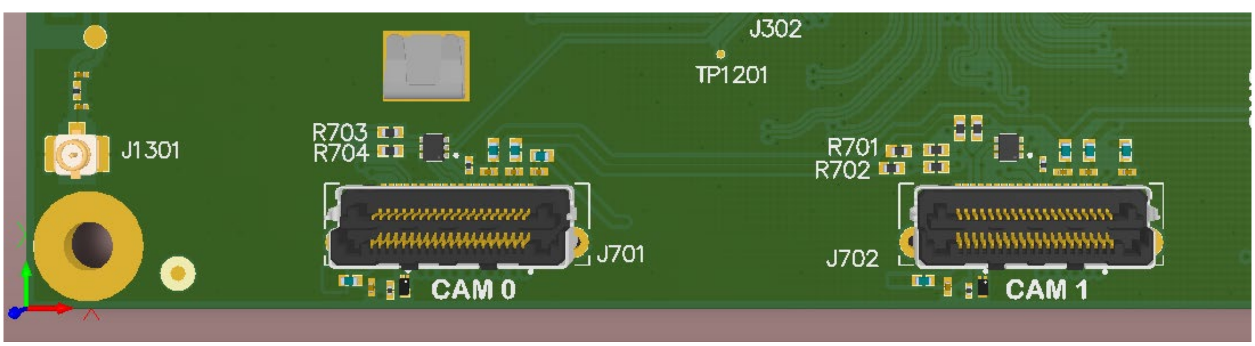

Figure 10 – MIPI CSI Camera Connectors on Rev 0100 CB

The table below describes the pin out for each connector. Signal directions listed are relative to the carrier board. Unless noted otherwise, single ended signals are referenced to +1.8V.

NOTE:

The MIPI CSI0 connector (J701) has a 4-lane MIPI interface, while the MIPI CSI1 connector (J702) is only has a 2-lane MIPI interface.

Table 4 – MIPI CSI Camera Connector Pinout (For Rev 0100)

Pin#	Signal Name (J701)	Signal Name (J702)	Description
1, 7, 13, 19, 25, 31, 4, 8, 12, 16, 24, 32, 38	GND	GND	Ground
3, 5	CSI0_CLK_N / P	CSI1_CLK_N	Input. MIPI CSI0 / CSI1 clock lane
9, 11	CSI0_LANE0_N / P	CSI1_LANE0_N / P	Input. MIPI CSI0 / CSI1 data lane 0
15, 17	CSI0_LANE1_N / P	CSI1_LANE1_N / P	Input. MIPI CSI0 / CSI1 data lane 1
21, 23	CSI0_LANE2_N / P	NC	Input. MIPI CSI0 data lane 2
27, 29	CSI0_LANE3_N / P	NC	Input. MIPI CSI0 data lane 3
33	CSI0_MCLK (APQ8016E GPIO26)	CSI1_MCLK (APQ8016E GPIO27)	Output. Camera master clock.
35	CSI0_RST (APQ8016E GPIO35)	CSI1_RST (APQ8016E GPIO28)	Output. Camera reset.
37, 39, 40	VPH_PWR_3P7	VPH_PWR_3P7	Power output. +3.7V.
2	VREG_L10_2P8	VREG_L10_2P8	Power output. Connected to PM8916 VREG_L10 LDO output. Default is +2.8V
6	VREG_L6_1P8	VREG_L6_1P8	Power output. Connected to PM8916 VREG_L6 LDO output. Default is +1.8V
10	VREG_L17_2P85	VREG_L17_2P85	Power output. Connected to PM8916 VREG_L17 LDO output. Default is +2.85V
18	CSI0_PWDN (APQ8016E GPIO34)	CSI0_PWDN (APQ8016E GPIO33)	Output. Camera power down.
20, 22	CCI0_I2C_SCL / SDA	CCI0_I2C_SCL / SDA	Camera CCI0 I2C clock interface
34, 36	BLSP6_0 / 1	BLSP6_0 / 1	Spare I2C port.
14, 26, 28, 30	NC	NC	Not connected.

4.5.2 Open-Q™ Carrier Board Rev 0200

The Rev 0200 Open-Q™ 410 carrier board has two MIPI CSI camera connectors: J1401 and J1501. The two JAE FI-RE41S-VF 41-pins connectors are shown in the figure below.

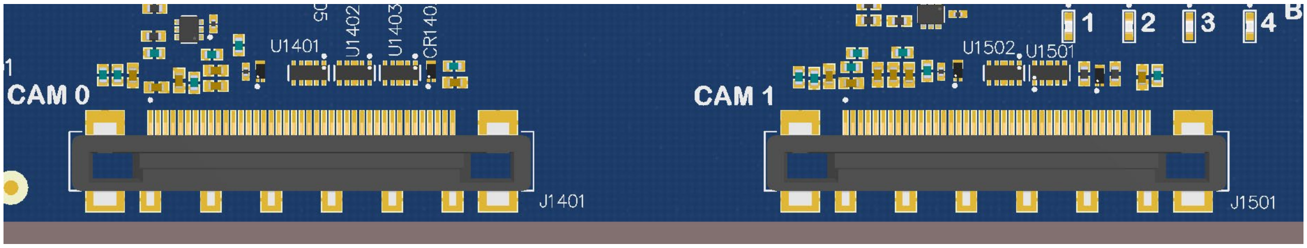

Figure 11 – MIPI CSI Camera Connectors on Rev 0200 CB

NOTE:
The MIPI CSI0 connector (J1401) has a 4-lane MIPI interface, while the MIPI CSI1 connector (J1501) only has a 2-lane MIPI interface.

Table 5 – MIPI CSI Camera Connector Pinout (For Rev 0200)

Pin #	J1401	J1501	Description
23/24	MIPI_CSI0_CLK_N/P	MIPI_CSI1_CLK_N/P	Input. MIPI CSI0 / CSI1 clock lane
20/21	MIPI_CSI0_LANE0_N/P	MIPI_CSI1_LANE0_N/P	Input. MIPI CSI0 / CSI1 data lane 0
26/27	MIPI_CSI0_LANE1_N/P	MIPI_CSI1_LANE1_N/P	Input. MIPI CSI0 / CSI1 data lane 1
29/30	MIPI_CSI0_LANE2_N/P	Not Available (N/C)	Input. MIPI CSI0 data lane 2
33/32	MIPI_CSI0_LANE3_N/P	Not Available (N/C)	Input. MIPI CSI0 data lane 3 ***This pair's order is swapped on purpose***
13	CSI0_RST_N (APQ8016E GPIO 35)	CSI1_RST_N (APQ8016E GPIO 28)	Output. Camera reset.
14	CSI0_PWDN	CSI1_PWDN	Output. Camera power down.

Pin #	J1401	J1501	Description
	(APQ8016E GPIO 34)	(APQ8016E GPIO 33)	
15	CCI0_I2C_SCL (APQ8016E GPIO 30)	CCI0_I2C_SCL (APQ8016E GPIO 30)	External PU to VREG_L6_1P8 through a 2K on Open-Q 410 CCB
16	CCI0_I2C_SDA (APQ8016E GPIO 29)	CCI0_I2C_SDA (APQ8016E GPIO 29)	External PU to VREG_L6_1P8 through a 2K on Open-Q 410 CCB
17	CSI0_MCLK (APQ8016E GPIO 26)	CSI1_MCLK (APQ8016E GPIO 27)	Output. Camera master clock.
36	BLSP6_0 (APQ8016E GPIO 23)	BLSP6_0 (APQ8016E GPIO 23)	External PU to VREG_L6_1P8 through a 2K on Open-Q 410 CCB
35	BLSP6_1 (APQ8016E GPIO 22)	BLSP6_1 (APQ8016E GPIO 22)	External PU to VREG_L6_1P8 through a 2K on Open-Q 410 CCB
7, 8	VREG_L10_2P8	VREG_L10_2P8	Default voltage: 2V8 Default usage: Camera AVDD
9, 10	VREG_L6_1P8	VREG_L6_1P8	Default voltage: 1V8 Default usage: Camera DVDD
5	VREG_L17_2P85	VREG_L17_2P85	Default voltage: 2V85 Default usage: Camera AVDD

Pin #	J1401	J1501	Description
1, 2, 3	VREG_3P3	VREG_3P3	Default voltage: 3V3 Default usage: Main system power rail.
6, 39	ELDO_CAM0_DVDD	ELDO_CAM1_DVDD	Default voltage: 1V12 Default usage: Digital Core VDD
40, 41	VREG_DBU4_5V	VREG_DBU4_5V	Default voltage: 5V0 (disconnected by default)
4, 11, 19, 22, 25, 28, 31, 34	GND	GND	
12, 18, 37, 38	No Connection	No Connection	These pins are not connected in the default configuration.

4.6 Display Connector

The Carrier board display connector (J801) provides the means for connecting the optional DSI display adapter assembly or the HDMI output adapter. The connector used is an FCI 60-pin 10106813-061112LF.

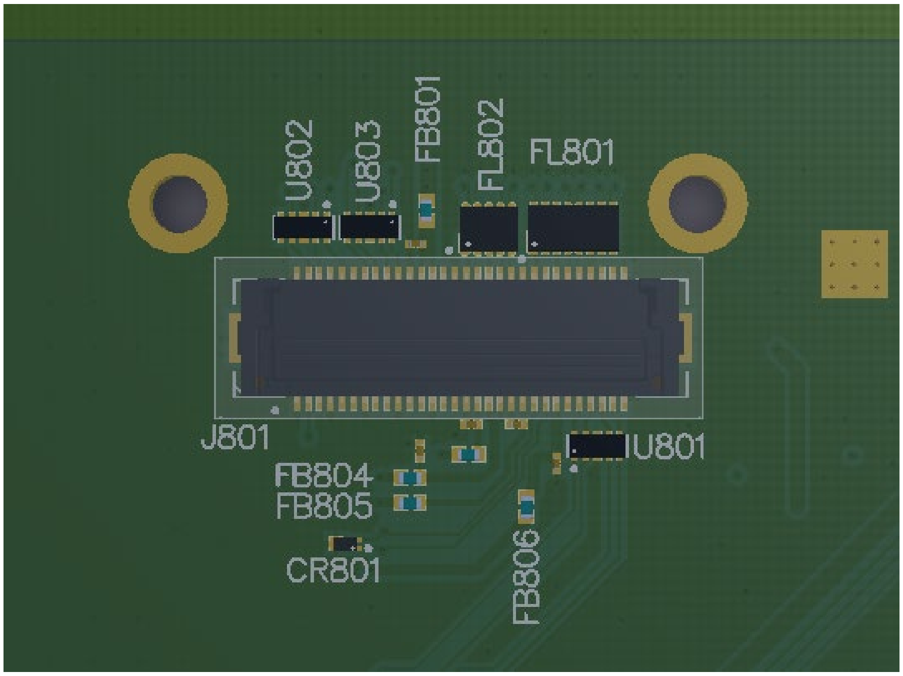

Figure 12 – Display Connector J801

The table below describes the pin out for the display connector. Signal directions listed are relative to the carrier board. Unless noted otherwise, single ended signals are referenced to +1.8V.

NOTE:

The Open-Q™ 410 Display Connector (J801) and mounting hole arrangement are physically compatible with the Dragonboard 800 Display , and the Open-Q™ 805 Display. Only display adapters labelled for use with the Open-Q™ 410 development kit should be connected. **Connecting the wrong display adapters may causes permanent damage to the hardware.**

Table 6 – Display Connector J801 Pinout

Pin No	Net	Description
1, 7, 13, 19, 25, 31, 39, 49, 59, 2, 12, 22, 30, 36, 42, 48, 54, 60	GND	Ground
3	BBCLK2	Clock output for HDMI Adapter board
33	VREG_L5_1P8	Power output from PM8916 VREG_L5 LDO. Default voltage is +1.8V.
35, 37	VREG_L17_2P85	Power output from PM8916 VREG_L17 LDO. Default voltage is +2.85V.
41	VREG_DBU4_5V	Power output from carrier board +5V buck regulator.
43	GP24_LCD_TE	APQ8016E GPIO24. Alternate function as vertical sync.
45	BLSP6_3	APQ8016E BLSP6 bit 3.
47	VREG_3P3	Power output from carrier board +3.3V LDO
51	GP32_DSI_SEL	APQ8016E GPIO32. Default use as display reset.
53	BLSP4_3_TS_RST	APQ8016E BLSP4 bit 3. Default use as touch screen reset.
55	BLSP4_2_TS_INT	APQ8016E BLSP4 bit 2. Default use as touch screen interrupt.
57	GP31_DSI_INT	APQ8016E GPIO31. Default use as display interrupt
4	GP118_MI2S_SCK	APQ8016E GPIO118. Alternate function as I2S.
6	GP25_LCD_RST_N	APQ8016E GPIO25. Default use as display reset.
10	MPP4_BL_CTRL	PM8916 MPP4. Default use as backlight control
14	GP119_MI2S_D0	APQ8016E GPIO119. Alternate function as I2S.
16	GP117_MI2S_WS	APQ8016E GPIO117. Alternate function as I2S.
18	BLSP4_1_I2C_SDA	APQ8016E BLSP4 bit 1. Default use as touch screen I2C.
20	BLSP4_0_I2C_SCL	APQ8016E BLSP4 bit 0. Default use as touch screen I2C.
24, 26	VPH_PWR_3P7	+3.7V power output
28	VREG_L6_1P8	Power output from PM8916 VREG_L6 LDO. Default voltage is +1.8V.
32, 34	DSI0_LANE2_FLT_N/P	MIPI DSI0 data lane2
40, 38	DSI0_LANE3_FLT_N/P	MIPI DSI0 data lane3
44, 46	DSI0_CLK_FLT_N/P	MIPI DSI0 clock
50, 52	DSI0_LANE0_FLT_N/P	MIPI DSI0 data lane0
56, 58	DSI0_LANE1_FLT_N/P	MIPI DSI0 data lane1
8, 5, 9, 11, 15, 17, 21, 23, 27, 29	NC	Not connected

4.7 USB Host / Device Connections

While the Open-Q™ 410 Development Kit provides a USB micro-B (device, J601) connector and a dual USB Type-A (host, J602) connector, the functionality of these connectors are mutually exclusive, with the USB micro-B connector taking priority.

NOTE:

DIP switch (S501) must be left in the OFF position. The selection for USB device or host is determined by the connectivity of the USB micro-B connector (J601) to an external USB host. If J601 is connected, the USB port operates as device mode. If J601 is not connected, the USB port operates as host mode on J602.

It is recommended to power down before switching the USB device / host capability.

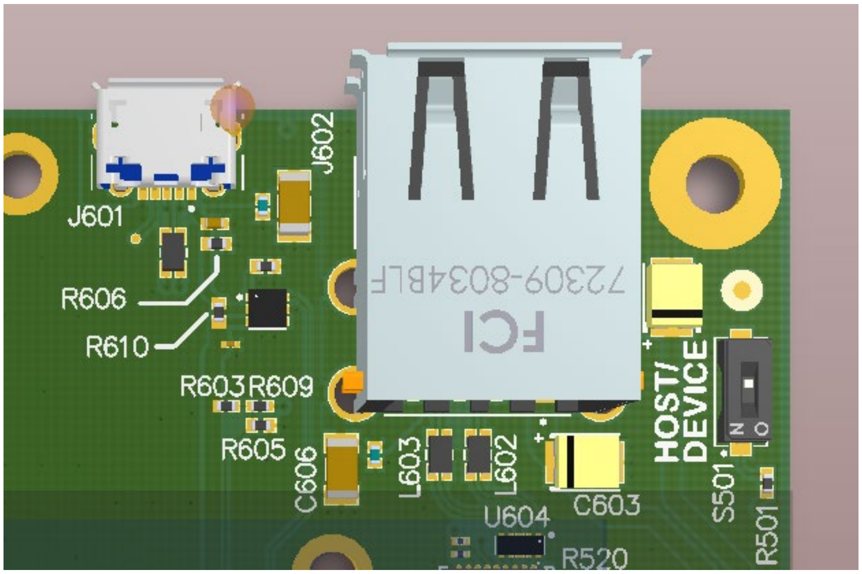

Figure 13 – USB Connections

4.8 Micro SD Socket

The Open-Q™ 410 Platform has a Micro SD push-push style socket connected to the SDC2 interface of the processor. The socket is found on the bottom side of the board as shown below.

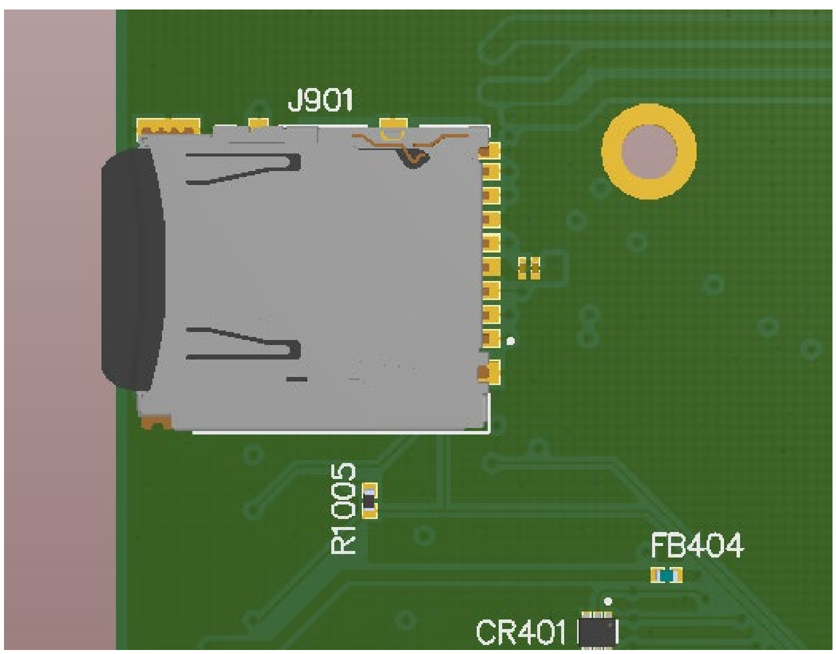

Figure 14 – Micro SD Socket, J901

4.9 Sensor Expansion Header

The Open-Q™ 410 Platform includes a 24-pin sensor expansion header (J1001). The header is a male, shrouded, 0.1" header as shown in the figure below.

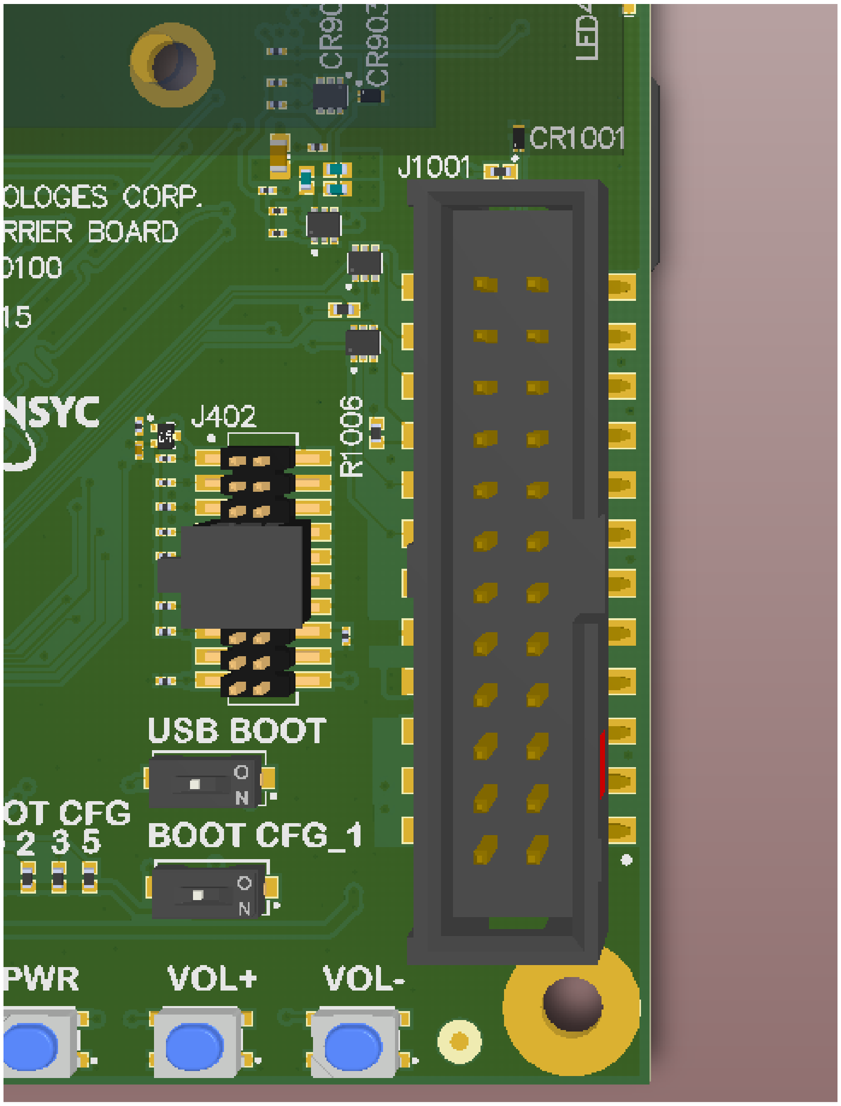

Figure 15 – Sensor Expansion Header

Since this connector contains power rails, GPIOs, and I2C lines, it can be used for purposes other than a sensor interface, such as connecting the Lantronix IoT development kit. The table below describes the pin-out for the sensor expansion header. Signal directions listed are relative to the carrier board. Unless noted otherwise, single ended signals are referenced to +1.8V. The pin 1 location on the header is indicated by the white dot in the lower right of the image above.

Table 7 – Sensor Expansion Header Pinout

Description	Signal Name	Pin #	Pin #	Signal Name	Description
Input / output. BLSP2 bit 1 I2C data signal. Connected to APQ8016E GPIO6.	BLSP21_I2C_SDA	1	2	GP110	Accelerometer interrupt input 1. Connected to APQ8016E GPIO110.
Output. BLSP2 bit 0 I2C clock signal. Connected to APQ8016E GPIO7.	BLSP20_I2C_SDC	3	4	GP114	Accelerometer interrupt input 2. Connected to APQ8016E GPIO114.
Output. Sensor reset signal. Connected to APQ8016E GPIO36.	GP36	5	6	GP115_GYRO_INT	Gyroscope interrupt input. Connected to APQ8016E GPIO115.
Power output. Connected to PM8916 VREG_L5 LDO output. Sensor IO voltage rail. Default is +1.8V.	VREG_L5_1P8	7	8	VREG_L17_2P85	Power output. Connected to PM8916 VREG_L17 LDO output. Sensor analog voltage rail. Default is +2.85V.
GND	GND	9	10	GND	GND
NC	NC	11	12	NC	NC
NC	NC	13	14	GP113_ALS_INT	Ambient light sensor interrupt input. Connected to APQ8016E GPIO113.
Connected to APQ8016E GPIO10 (BLSP 3 bit 1).	BLSP31	15	16	GP69_MAG_INT	Magnetometer interrupt input. Connected to APQ8016E GPIO69.
NC	NC	17	18	BLSP30	Pressure sensor interrupt input. Connected to APQ8016E BLSP3 bit 0.
Connected to APQ8016E GPIO18 (BLSP 5 bit 1). Can be used as I2C SDA.	BLSP51	19	20	BLSP53	Connected to APQ8016E BLSP5 bit 3.
Connected to APQ8016E GPIO19 (BLSP 5 bit 0). Can be used as I2C SCL.	BLSP50	21	22	BLSP52	Connected to APQ8016E BLSP5 bit 2.
Connected to APQ8016E GPIO9 (BLSP 3 bit 2).	BLSP32	23	24	BLSP33	Connected to APQ8016E BLSP3 bit 3.

4.10 JTAG Header

Note: There is no software support for JTAG

The Open-Q™ 410 Platform includes a 20-pin JTAG header (J602). The header is a male, keyed, 0.05" header as shown in the figure below. Part number is SAMTEC FTSH-110-01-L-DV-K-P. This JTAG header is intended to be used with a Lauterbach 20-pin JTAG module. A conversion cable is required to connect the 0.05" pitch JTAG header to the 0.1" pitch JTAG module.

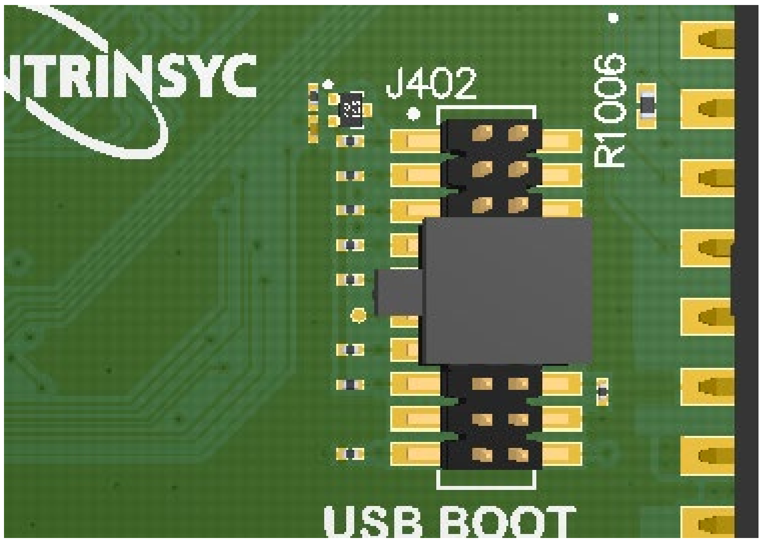

Figure 16 – JTAG Header

The table below describes the pin-out for the JTAG header. Signal directions listed are relative to the carrier board. Unless noted otherwise, single ended signals are referenced to +1.8V.

Table 8 – JTAG Header Pinout

Description	Signal Name	Pin #	Pin #	Signal Name	Description
Output. Connected to PM8916 VREG_L5 +1.8V regulator when JTAG module presence is detected via pin 20.	JTAG_PS_HOLD	1	2	GND	GND
Input. Connected to APQ8016E TRST_N pin.	JTAG_TRST_N	3	4	GND	GND
Input. Connected to APQ8016E TDI pin.	JTAG_TDI	5	6	GND	GND
Input. Connected to APQ8016E TMS pin.	JTAG_TMS	7	8	GND	GND
Input. Connected to APQ8016E TCK pin.	JTAG_TCK	9	10	GND	GND

Description	Signal Name	Pin #	Pin #	Signal Name	Description
NC. Connected to test point TP601.	JTAG_RTCK	11	12	GND	GND
Output. Connected to APQ8016E TDO pin.	JTAG_TDO	13	14	GND	GND
Input. Connected to APQ8016E SRST_N pin.	JTAG_SRST_N	15	16	GND	Pulled to GND via 4.7K resistor.
NC	NC	17	18	GND	GND
Pulled to GND via 4.7K resistor.	GND	19	20	JTAG_DET_N	Input. Connected to GND by JTAG module. Used to detect the presence of a connected JTAG module.

4.11 Audio Connectors

The Open-Q™ 410 Development Kit has several audio connectors that are described in this section. The audio codec functionality is contained with the APQ8016E CPU and PM8916 PMIC. The table below describes the audio path routing on the Open-Q™ 410 development kit.

Table 9 – Audio Path Connections

Function	Signal Name	Description
Digital MIC	DMIC0_CLK/DATA	Connected to Digital Mic Header (J1104). Also usable as BLSP1.
MIC1 Input	CDC_MIC1_P	Connected to Stereo Line Input jack (J1101)
MIC2 Input	CDC_MIC2_P	Connected to Headset jack (J1105)
MIC3 Input	CDC_MIC3_P	Connected to Stereo Line Input jack (J1101)
Earpiece Output	CDC_EAR_N/P	Connected to speaker connector (J1102).
Headphone Stereo Output	CODEC_FLT_HPH_L	Connected to Headset jack (J1105)
Speaker Output (Class D)	SPKR_OUT_N/P	Connected to speaker connector (J1103).

4.11.1 Audio 3.5mm Jacks

There are two 3.5mm audio jacks on the carrier board as shown below. Connector J1105 is configured for use with a typical TRRS Android headset jack. Connector J1101 is wired for use as a stereo line input.

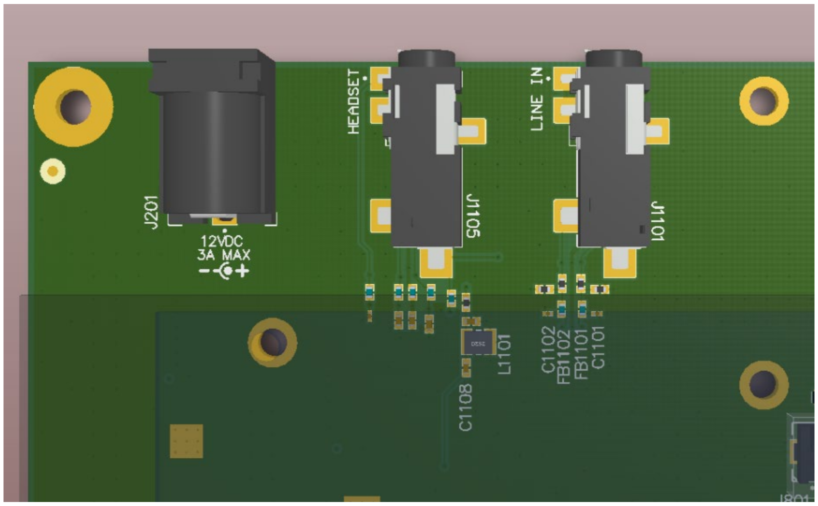

Figure 17 – Audio 3.5mm Jacks

4.11.2 Speaker Connectors

There are two, 2-pin speaker connectors on the carrier board as shown below. Connector J1102 is for the earpiece audio output. Connector J1103 is for the loud speaker output. Both connectors are of type JST B2B-PH-SM4-TB(LF)(SN).

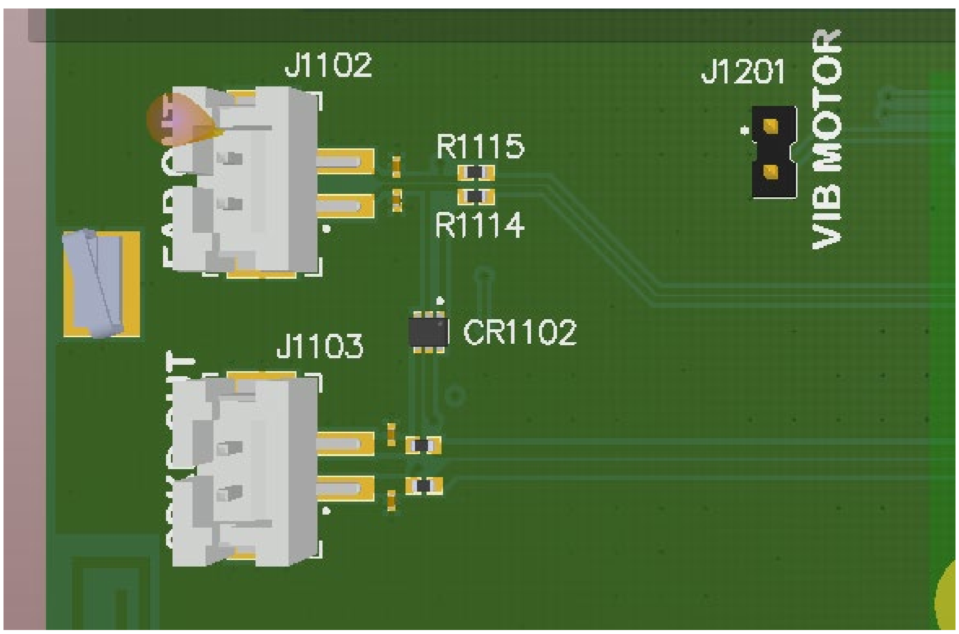

Figure 18 – Speaker Connectors

The pinout for the speaker connectors is shown below.

Table 10 – Speaker Connector Pinout

Pin #	J1102 Signal Name	J1103 Signal Name	Description
1	CDC_EAR_N	SPKR_OUT_N	Audio output negative.
2	CDC_EAR_P	SPKR_OUT_P	Audio output positive.

4.11.3 Digital Mic Header

J1104 is a 6-pin header (see below) that contains connections from BLSP1 on the CPU. These connections also double as a digital microphone input. The header is found on the bottom side of the carrier board.

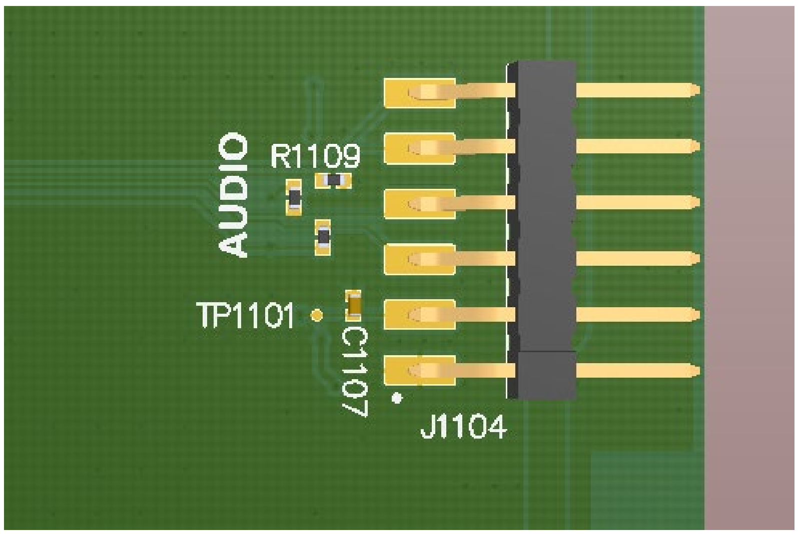

Figure 19 – Digital Mic Header

The pinout for the digital Mic header is shown below.

Table 11 – Digital Mic Header Pinout

Pin #	J1104 Signal Name	Description
1	GND	Ground
2	CDC_MIC_BIAS1	Digital Mic VDD
3	BLSP10	CPU BLSP1 bit 0.
4	BLSP11	CPU BLSP1 bit 1.
5	BLSP12_DMIC_DAT	CPU BLSP1 bit 2. Can be configured for digital Mic data line.
6	BLSP13_DMIC_CLK	CPU BLSP1 bit 3. Can be configured for digital Mic clock line.

4.12 Other Interfaces

J1201 is a 2-pin header found next to the speaker connectors that can be used to drive a vibrator motor if desired. See the speaker connector figure above for the location of the header.

4.13 System Auto Boot

The system can auto boot-up by:

1. Install R1209 (0Ω). (Pulling CBL_PWR_N to GND)
2. Set the device into device mode (Only required for Rev 0100)
3. Connect the development kit to a PC through J601 (ADB port, not serial debug)

5 Output Display Options

The Open-Q™ 410 development kit can be purchased with two output display options: an on-board display or an HDMI output. Both of these options are connected to the carrier board display connector described above.

Please visit: http://shop.intrinsyc.com/collections/dragonboard-accessories for more information.

5.1 On-Board Display

There are two optional on-board displays supported by the Open-Q 410:

1. 4.46" FWVGA MIPI DSI LCD (Manufactured by Truly) with capacitive multi-touch
2. 4.5" FWVGA MIPI DSI LCD (Manufactured by OSD Displays) with capacitive multi-touch

Option 1: 4.46" panel manufactured by Truly, with an integrated capacitive touch panel. Detailed specifications of this display board:

- Model No: TDO-FWVGA0446G00002
- Resolution: FWVGA (480x854xRGB)
- Display Controller: Himax HX83796C
  - Support DSI Version 1.10
  - Support D-PHY version 1.10
- Touch Controller: Synaptic S3202 Multi Touch Capacitive with HW buttons
- Interface: MIPI DSI (2 data lanes)

Figure 20 – Truly FWVGA Panel

Option 2: 4.5” panel manufactured by OSD Displays, with an integrated capacitive touch panel. Detailed specifications of this display board:

- Model No: OSD045T2906-43TS
- Resolution: FWVGA (480x854xRGB)
- Display Controller: Fitipower Integrated Technology JD9161BA
    - Support DSI Version 1.1
    - Support D-PHY version 1.00
- Touch Controller: GoodixSilited GSL968 Multi Touch Capacitive
- Interface: MIPI DSI (2 data lanes)

5.2 HDMI Output Adapter

The optional HDMI output adapter board can be used in place of the on-board display. The image below shows the HDMI output adapter installed on the development kit.

There is a standard HDMI 1.4 Type A connector on a top left corner of the carrier board after the HDMI output adapter installed.

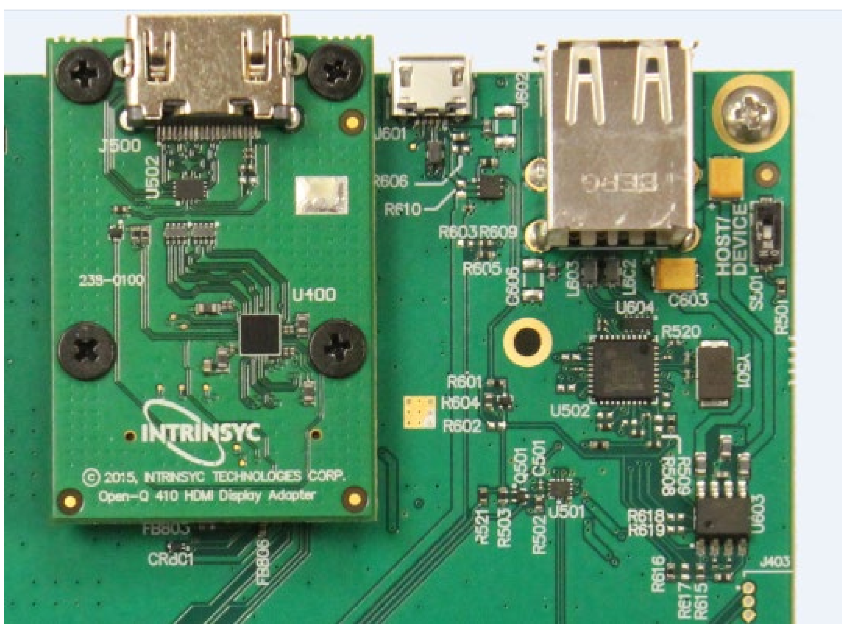

Figure 21 – HDMI Output Adapter