

Open-Q 845 μ SOM Hardware Datasheet

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Revision History

Date	Rev.	Comments
July 2019	1.0	Initial Release – Preliminary – subject to change Intrinsyc document number: ITC-01DEV1430-SOM-DS Intrinsyc document title: Open-Q 845 uSOM Hardware Device Specification
August 2019	1.1	Preliminary – subject to change <ul style="list-style-type: none">Removed FLASH_LED3 from pin listRemoved GPIO_133_BOOTCFG_3 from listAdded HAPT_PWM_IN to the pin listAdded GPIO25_OIS_SYNC to the pin list
August 2019	1.2	Preliminary – subject to change <ul style="list-style-type: none">Changed SOM image to 845 uSOM CAD imageRevised a GPIO description
August 2019	1.3	Preliminary – subject to change <ul style="list-style-type: none">Added SOM B2B connector pinoutAdded pin definition to interface tables
August 2019	1.4	Preliminary – subject to change <ul style="list-style-type: none">Swapped JT1 pin71 SSC6_QUP1_4_SPI1_CS1_N with JT2 pin99 SSC8_QUP2_0_SPI2_MISO
September 2019	1.5	Document cleanup and updated images. Removed redundant pinout tables – see CB Design Guide doc for more pin description details.
November 2019	1.6	<ul style="list-style-type: none">Updated SOM operating temperature range.Removed preliminary notes and updated images.
February 2020	1.7	<ul style="list-style-type: none">Added partial power consumption numbers to section 5.4.
July 2020	A	Initial Lantronix document. Added Lantronix document part number, Lantronix logo, branding, contact information, and links.

For the latest revision of this product document, please go to: <http://tech.intrinsyc.com>.

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1. Introduction

This document applies to the Open-Q 845 μ SOM. Technical specifications for other SOMs in the Lantronix product line are covered under separate documents.

1.1 Purpose

The purpose of this document is to provide the technical specifications of the Lantronix Open-Q 845 μ SOM.

1.2 Scope

This document covers the following information on the Open-Q 845 μ SOM:

- Electrical and mechanical specifications
- SOM pin-out
- Device handling and packaging
- Ordering information.

1.3 Intended Audience

This document is intended for users who wish to understand the technical specifications of the Lantronix Open-Q 845 μ SOM.

1.4 Acronyms and Abbreviations

Acronym / Abbreviation	Definition
ANT	ANTenna
BAT, BATT	BATTery
BAM	Bus Access Manager
BLSP	BAM-based Low-Speed Peripheral
BOM	Bill Of Materials
BT	Blue Tooth
CLK	Clock
CPU	Central Processing Unit
CS	Chip Select
CSI	Camera Serial Interface
DSI	Display Serial Interface
EMI	Electro-Magnetic Interference
EN	ENable
ERM	Eccentric Rotating Mass
ESD	Electro-Static Discharge
GND	GrouND
GPIO	General Purpose I/O
GPS	Global Positioning System
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
INT	INTerrupt
JTAG	Joint Test Action Group

Acronym / Abbreviation	Definition
LDO	Low Drop-Out
LRM	Linear Resonant Actuator
LTE	Long-Term Evolution
LPI	Low Power Island
MDP	Mobile Display Port
MI2S	Mobile Inter-IC Sound
MIC	MICrophone
MIPI	Mobile Industry Processor Interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
PCB	Printed Circuit Board
PCIE	Peripheral Component Interconnect Express
PWM	Pulse-Width Modulation
QUP	Qualcomm Universal Peripheral
RF	Radio Frequency
RX	Receive
SCL	Serial Clock
SDA	Serial DATA
SDC	Secure Digital Interface
SOM	System On Module
SPI	Serial Peripheral Interface
SSC	Snapdragon Sensor Core
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UIM	User Interface Module
USB	Universal Serial Bus
WLAN	Wireless Local Area Network

1.5 Signal Name Suffix

Suffix	Definition
_N	Indicates that the signal is ACTIVE LOW
_P/N	Identifies the two signals comprising a differential pair

2. Documents

This section lists any parent and supplementary documents for the Open-Q 845 μ SOM Device Specification. Unless stated otherwise, applicable documents supersede this document and reference documents provide background and supplementary information.

2.1 Applicable Documents

REFERENCE	AUTHOR	TITLE
A-1	Intrinsyc	Intrinsyc Purchase and Software License Agreement for the Open-Q 845 μ SOM

2.2 Reference Documents

Available at <http://tech.intrinsyc.com> (dev kit registration required).

REFERENCE	TITLE
R-1	Open-Q 845 μ SOM Development Kit – User Guide
R-2	Open-Q 845 μ SOM – Carrier Board Design Guide
R-3	Open-Q 845 μ SOM Schematics (SOM and Carrier)

3. Summary of Features

The Open-Q 845 μ SOM contains the core of the Snapdragon 845 architecture. Measuring in at 50mm x 25mm, the SOM is where all the processing occurs. It connects to a carrier board via three 100 pin Hirose DF40 connectors which allows essential power rails and signals to be exposed for supporting peripherals and interfaces on the platform.

3.1 SOM Block Diagram

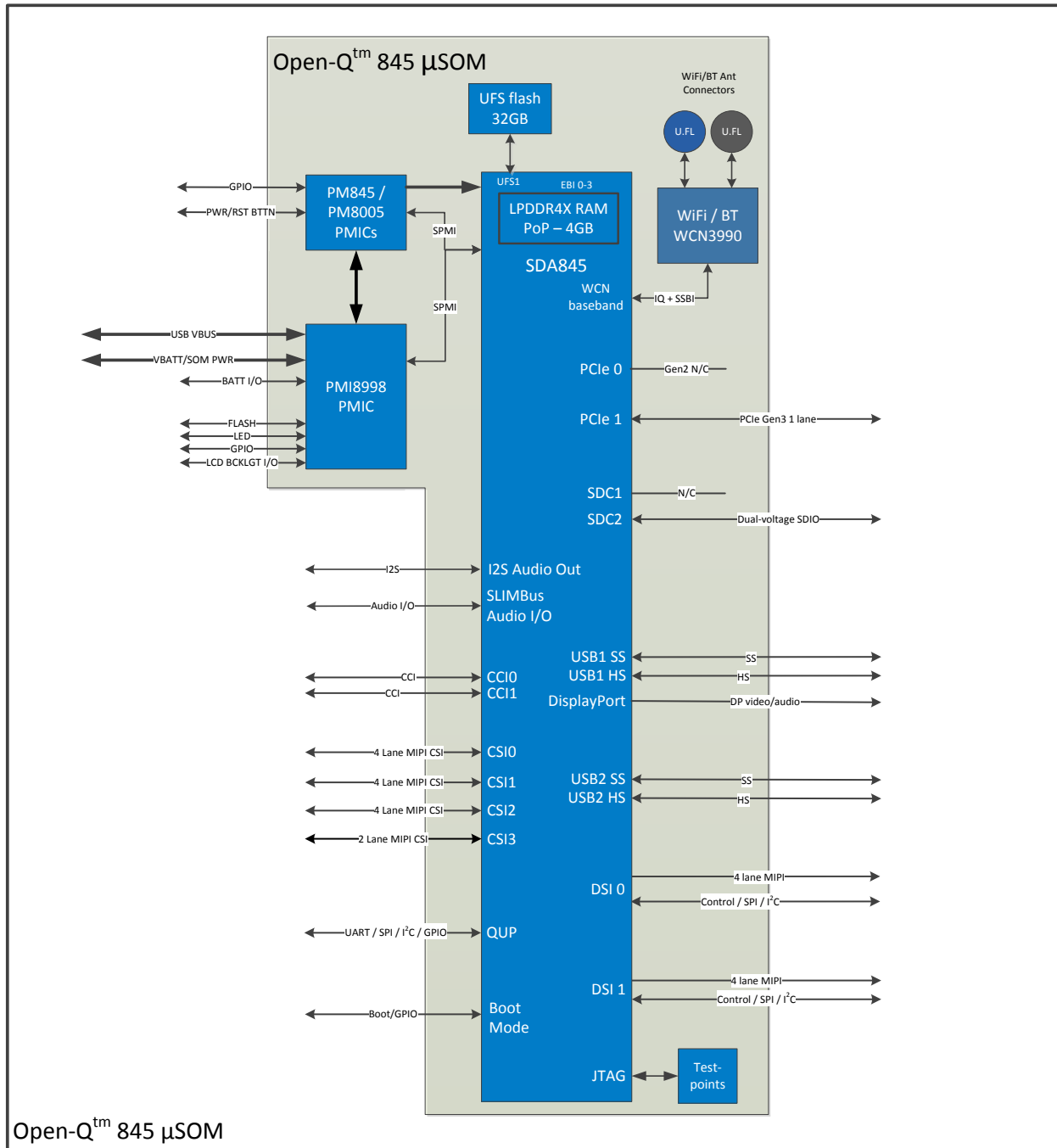


Figure 1 – Open-Q 845 μ SOM Block Diagram

3.2 SOM Technical Specifications

See the table below for the Open-Q 845 μ SOM technical specifications.

Table 1 – Open-Q 845 μ SOM Technical Specifications

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	SDA845 CPU	Qualcomm Snapdragon 845 Processor	Qualcomm® Kryo™ 385 CPU, 64-bit quad core, 2.649 GHz
			Qualcomm® Kryo™ Low Power, quad core, 1.766 GHz
	PMI8998 PMIC	Qualcomm PMIC for 845 Processor	Power management, battery charging, general housekeeping, user interface, and IC level interface support
	PM845 PMIC	Qualcomm master PMIC for 845 Processor	Power management, general housekeeping, IC level interface support
	PM8005 PMIC	Qualcomm Companion PMIC for 845 Processor	Power management, general housekeeping
Memory	SDRAM Memory	4GB PoP LPDDR4X memory	4x 16-bit LPDDR4X SDRAM 1866 MHz
	Flash Memory	Minimum 32GB UFS	UFS 2.1, 2x lane
Connectivity	Wi-Fi 5GHz/2.4GHz	Qualcomm WCN3990 WLAN / Bluetooth Wireless Connectivity IC	2x2 MIMO WLAN compliant with IEEE802.11 a/b/g/n/ac
	Bluetooth 2.4 GHz	Qualcomm WCN3990 WLAN / Bluetooth Wireless Connectivity IC	Compliant with Bluetooth version 5.0
RF Interfaces (see section below)	WLAN / BT	2 antenna connectors on SOM for 2x2 MIMO Wi-Fi. Bluetooth uses one of the 2 antenna ports.	2 x U.FL, 50 ohm coaxial connectors
Audio Interfaces	Digital MI2S	Three MI2S ports	One 4-bit port plus two additional ports multiplexed with Slimbus channel
	SLIMBUS	2 bit SLIMBUS port	Support for external audio codec

Subsystem / Connectors	Feature Set	Description	Specification
Digital Interfaces	MIPI CSI	Three 4-lane MIPI CSI Camera interfaces One 2-lane MIPI CSI Camera interface	4-lane supporting (4/4/4/2) D-PHY 1.2 (2.5 Gbps / lane) 2-lane supporting (4/4/4/2) D-PHY (2.5 Gbps / lane) Up to 32 MP 30fps dual ISP
	MIPI DSI	Two 4-lane MIPI DSI Display interfaces	Supporting D-PHY 1.2 (2.5 Gbps / lane) and 4K60
	USB	One USB 3.1 Type-C One USB 3.1 Type-A	USB Type-C includes DisplayPort 1.4 + data concurrency over USB
	PCIe	PCIe Gen 3	One Gen 3 1-lane with PHY 3.0
	SDIO	One 4-bit Secure Digital interface	SD v3.0, dual voltage interface
	GPIO / I2C / SPI / UART	Configurable IO	Configurable IO exposed as GPIO or QUP ports, giving GPIO, I2C, SPI, and UART connections options.
Connectors	3x 100-pin board to board connectors	3x Hirose 100-pin DF40C header connectors	300 pins total for connection to carrier board

4. I/O Definitions

4.1 Location of Major Components

The figures below identify the major components and connectors found on the Open-Q 845 μ SOM top and bottom sides.

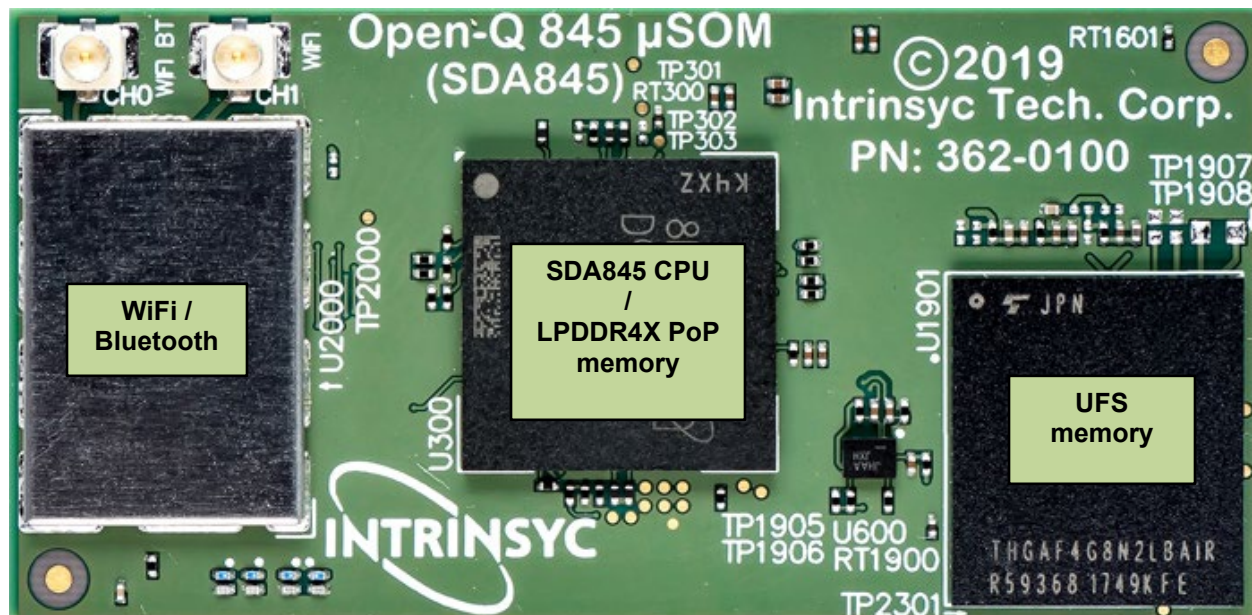


Figure 2 – Open-Q 845 μ SOM Top View

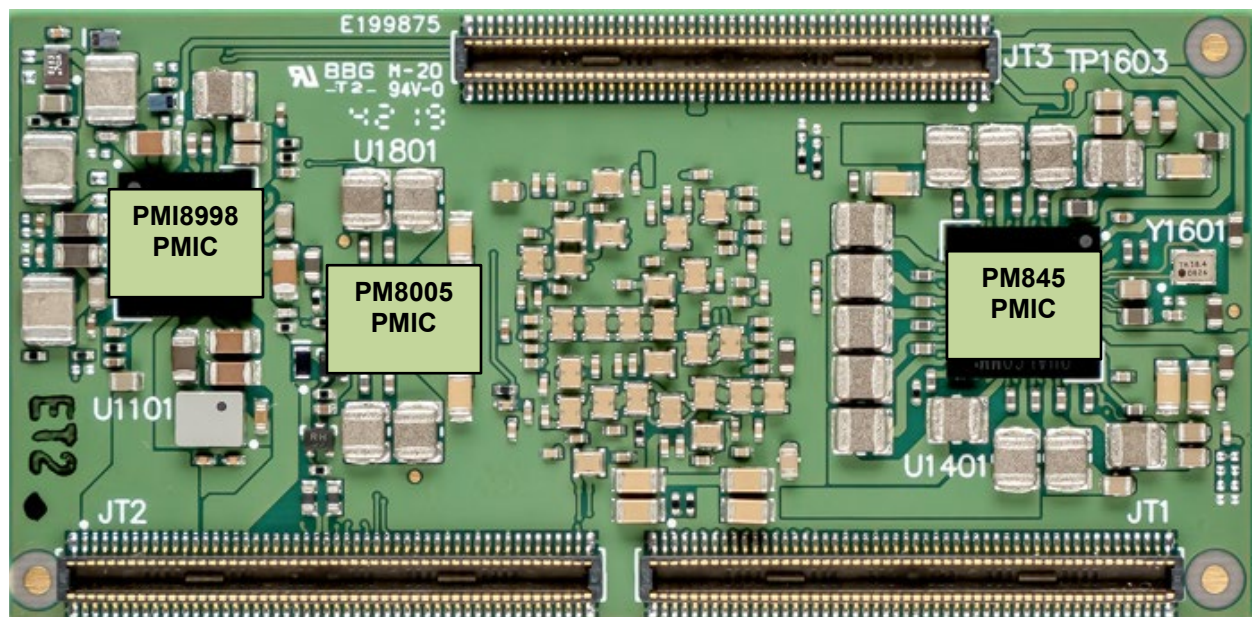


Figure 3 – Open-Q 845 μ SOM Bottom View

The SOM mating connectors JT1, JT2, and JT3 are located on the bottom side of the SOM. The connector pin 1 locations are shown in the figure below (looking at bottom of SOM). Key dimensions are provided in later sections of this document.

The connectors are Hirose DF40C-100DP-0.4V(51). See section 6.3 for information on the available mating connectors.

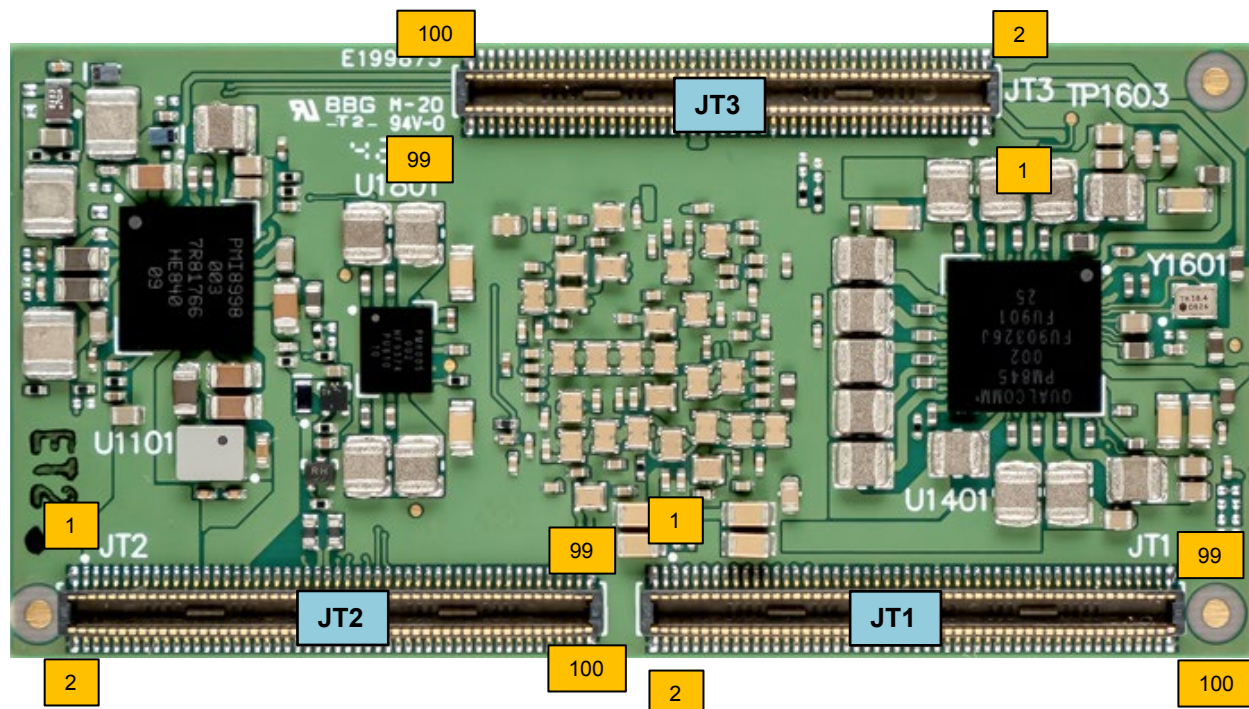


Figure 4 – Pin Locations of Board-to-Board Connectors

4.2 B2B Connector Signal Assignments

The following tables list the pin-outs of the three Open-Q 845 μ SOM board to board connectors. A more detailed description of the signal group functions follows in the sections below. These descriptions provide the background information for customers developing a custom Carrier Board for the Open-Q 845 μ SOM.

- Note: the SOM schematic (document R-3) is the controlling document. In the event of pin-out difference(s) between this document and the SOM schematic, the SOM schematic shall take precedence.

Table 2 – B2B Connector JT1 Pin-outs

Pin #	JT1 Signal Name	Description
1	GND	Ground reference for the SOM.
2	GND	Ground reference for the SOM.
3	MIPI_CSI1_CLK_P	MIPI camera serial interface 1 clock
4	MIPI_CSI3_CLK_P	MIPI camera serial interface 3 clock
5	MIPI_CSI1_CLK_N	MIPI camera serial interface 1 clock
6	MIPI_CSI3_CLK_N	MIPI camera serial interface 3 clock
7	GND	Ground reference for the SOM.

Pin #	JT1 Signal Name	Description
8	GND	Ground reference for the SOM.
9	MIPI_CSI1_LANE0_P	MIPI camera serial interface 1 data
10	MIPI_CSI3_LANE0_N	MIPI camera serial interface 3 data
11	MIPI_CSI1_LANE0_N	MIPI camera serial interface 1 data
12	MIPI_CSI3_LANE0_P	MIPI camera serial interface 3 data
13	GND	Ground reference for the SOM.
14	GND	Ground reference for the SOM.
15	MIPI_CSI1_LANE1_P	MIPI camera serial interface 1 data
16	MIPI_CSI3_LANE1_P	MIPI camera serial interface 3 data
17	MIPI_CSI1_LANE1_N	MIPI camera serial interface 1 data
18	MIPI_CSI3_LANE1_N	MIPI camera serial interface 3 data
19	GND	Ground reference for the SOM.
20	GND	Ground reference for the SOM.
21	MIPI_CSI1_LANE2_P	MIPI camera serial interface 1 data
22	MIPI_CSI0_CLK_N	MIPI camera serial interface 0 clock
23	MIPI_CSI1_LANE2_N	MIPI camera serial interface 1 data
24	MIPI_CSI0_CLK_P	MIPI camera serial interface 0 clock
25	GND	Ground reference for the SOM.
26	GND	Ground reference for the SOM.
27	MIPI_CSI1_LANE3_P	MIPI camera serial interface 1 data
28	MIPI_CSI0_LANE0_P	MIPI camera serial interface 0 data
29	MIPI_CSI1_LANE3_N	MIPI camera serial interface 1 data
30	MIPI_CSI0_LANE0_N	MIPI camera serial interface 0 data
31	GND	Ground reference for the SOM.
32	GND	Ground reference for the SOM.
33	MIPI_CSI2_LANE3_P	MIPI camera serial interface 2 data
34	MIPI_CSI0_LANE1_P	MIPI camera serial interface 0 data
35	MIPI_CSI2_LANE3_N	MIPI camera serial interface 2 data
36	MIPI_CSI0_LANE1_N	MIPI camera serial interface 0 data
37	GND	Ground reference for the SOM.
38	GND	Ground reference for the SOM.
39	MIPI_CSI2_LANE2_N	MIPI camera serial interface 2 data
40	MIPI_CSI0_LANE2_P	MIPI camera serial interface 0 data
41	MIPI_CSI2_LANE2_P	MIPI camera serial interface 2 data
42	MIPI_CSI0_LANE2_N	MIPI camera serial interface 0 data
43	GND	Ground reference for the SOM.
44	GND	Ground reference for the SOM.
45	MIPI_CSI2_LANE1_N	MIPI camera serial interface 2 data
46	MIPI_CSI0_LANE3_N	MIPI camera serial interface 0 data
47	MIPI_CSI2_LANE1_P	MIPI camera serial interface 2 data

Pin #	JT1 Signal Name	Description
48	MIPI_CSIO_LANE3_P	MIPI camera serial interface 0 data
49	GND	Ground reference for the SOM.
50	GND	Ground reference for the SOM.
51	MIPI_CSI2_LANE0_P	MIPI camera serial interface 2 data
52	GPIO24_CAM_IRQ	Camera interrupt input / Configurable GPIO
53	MIPI_CSI2_LANE0_N	MIPI camera serial interface 2 data
54	GPIO40_W_DISABLE_N	PCIE Gen3 Port 1 – wireless disable signal / Configurable GPIO
55	GND	Ground reference for the SOM.
56	GPIO23_CAM3_RST_N	Camera 3 reset output / Configurable GPIO
57	MIPI_CSI2_CLK_N	MIPI camera serial interface 2 clock
58	GPIO13_CAM_MCLK0	Camera master clock 0 / Configurable GPIO
59	MIPI_CSI2_CLK_P	MIPI camera serial interface 2 clock
60	GPIO14_CAM_MCLK1	Camera master clock 1 / Configurable GPIO
61	GND	Ground reference for the SOM.
62	VOL_UP_N	PM845 GPIO_06 volume up button input / Configurable GPIO
63	GPIO132_USR_BTN	General purpose user button input / Configurable GPIO
64	CBL_PWR_N	Optional input that, when grounded, can initiate an auto power on sequence.
65	SSC5_QUP1_3_SPI1_CS0_N	Snapdragon sensor core SPI 1
66	GPIO18_CCI_I2C_SCL0	Camera control interface 0 I2C / Configurable GPIO
67	SSC1_QUP0_1_I2C1_SCL	Snapdragon sensor core I2C 1
68	GPIO17_CCI_I2C_SDA0	Camera control interface 0 I2C / Configurable GPIO
69	SSC0_QUP0_0_I2C1_SDA	Snapdragon sensor core I2C 1
70	GPIO15_CAM_MCLK2	Camera master clock 2 / Configurable GPIO
71	SSC8_QUP2_0_SPI2_MISO	Snapdragon sensor core SPI 2
72	GPIO25_OIS_SYNC	Camera timer / Camera asynchronous IO / Configurable GPIO
73	SSC11_QUP2_3_SPI2_CS_N	Snapdragon sensor core SPI 2
74	GND	Ground reference for the SOM.
75	SSC9_QUP2_1_SPI2_MOSI	Snapdragon sensor core SPI 2
76	GPIO16_CAM_MCLK3	Camera master clock 3 / Configurable GPIO
77	SSC10_QUP2_2_SPI2_CLK	Snapdragon sensor core SPI 2
78	GPIO20_CCI_I2C_SCL1	Camera control interface 1 I2C / Configurable GPIO

Pin #	JT1 Signal Name	Description
79	PM_RESIN_VOLDN_N	Input typically connected to volume down user button that, when held low, can also be used for as reset input.
80	GPIO19_CCI_I2C_SDA1	Camera control interface 1 I2C / Configurable GPIO
81	GPIO117_ACCEL_INT	Sensor interrupt input / Configurable GPIO
82	SDC2_DATA3	Secure Digital IO data
83	GPIO118_GYRO_INT	Sensor interrupt input / Configurable GPIO
84	SDC2_DATA2	Secure Digital IO data
85	GPIO119_MAG_INT_N	Sensor interrupt input / Configurable GPIO
86	SDC2_DATA1	Secure Digital IO data
87	GPIO120_ALSP_INT_N	Sensor interrupt input / Configurable GPIO
88	SDC2_DATA0	Secure Digital IO data
89	GPIO144_WLAN_COEX_UART_TXD	Mini PCIe wireless coexistence UART / Configurable GPIO
90	SDC2_CMD	Secure Digital IO command
91	GPIO145_WLAN_COEX_UART_RXD	Mini PCIe wireless coexistence UART / Configurable GPIO
92	SDC2_CLK	Secure Digital IO clock
93	GPIO101_WDOG_DISABLE	Boot Configuration bit 0 (Watchdog Disable) input during power on sequence. Configurable GPIO at other times.
94	VREG_S4A_1P8	PM845 SMPS S4A +1.8V power output from SOM. Typically used for IO voltage and low current digital peripherals on the carrier board. While shared with SOM peripherals, it is expected that up to 600mA is available for carrier board usage.
95	VREG_LVS2A_1P8	PM845 LVS2A +1.8V low voltage switch output from SOM. Used for sensor IO voltage connections on the carrier board. 100mA is expected to be available for carrier board usage.
96	VREG_S4A_1P8	See JT1 pin 96
97	VREG_LVS1A_1P8	PM845 LVS1A +1.8V low voltage switch output from SOM. Used for camera IO voltage connections on the carrier board. 300mA is expected to be available for carrier board usage.

Pin #	JT1 Signal Name	Description
98	VREG_L22A_2P85	PM845 LDO 22A +2.85V power output from SOM. Can be used for other camera applications on the carrier board. 150mA is expected to be available for carrier board usage.
99	GPIO53_CODEEC_INT2_N	Audio codec interrupt input / Configurable GPIO
100	VREG_L28A_3P0	PM845 LDO 28A +3.0V power output from SOM. Can be used for display AVDD connections on the carrier board. 150mA is expected to be available for carrier board usage.

Table 3 – B2B Connector JT2 Pin-outs

Pin #	JT2 Signal Name	Description
1	SOM_SYS_PWR	Main power source for SOM. Single cell Lithium battery connection or 3.8V DC power input.
2	GND	Ground reference for the SOM.
3	SOM_SYS_PWR	See JT2 pin 1
4	GND	Ground reference for the SOM.
5	SOM_SYS_PWR	See JT2 pin 1
6	SOM_SYS_PWR	See JT2 pin 1
7	SOM_SYS_PWR	See JT2 pin 1
8	SOM_SYS_PWR	See JT2 pin 1
9	SOM_SYS_PWR	See JT2 pin 1
10	SOM_SYS_PWR	See JT2 pin 1
11	SOM_SYS_PWR	See JT2 pin 1
12	SOM_SYS_PWR	See JT2 pin 1
13	SOM_SYS_PWR	See JT2 pin 1
14	SOM_SYS_PWR	See JT2 pin 1
15	SOM_SYS_PWR	See JT2 pin 1
16	CS_P	Battery current sense resistor input for connection to battery plus terminal.
17	SOM_SYS_PWR	See JT2 pin 1
18	CS_N	Battery current sense resistor input for connection to battery minus terminal.
19	SOM_SYS_PWR	See JT2 pin 1
20	BATT_ID	Battery identification input that can be used for missing battery detection and charger enable / disable.
21	SOM_SYS_PWR	See JT2 pin 1
22	VBATT_CONN_VSENSE_N	Battery voltage sense input for connection to battery minus terminal.

Pin #	JT2 Signal Name	Description
23	SOM_SYS_PWR	See JT2 pin 1
24	VBATT_CONN_VSENSE_P	Battery voltage sense input for connection to battery plus terminal.
25	USB_VBUS	USB Type-C VBUS connection. When used as power input, this is the charge power source for battery powered applications. For USB host mode applications, this is a power output.
26	AUX_THERM	Auxiliary temperature input to PMIC ADC typically connected to remote thermistor located in 'quiet' area of carrier board.
27	USB_VBUS	See JT2 pin 25
28	BATT_THERM	Battery thermistor input used for measuring battery pack temperature for safe charger operation.
29	USB_VBUS	See JT2 pin 25
30	PHONE_ON_N	Input typically connected to keypad power-on button that, when grounded, can initiate a power on sequence or reset.
31	USB_VBUS	See JT2 pin 25
32	GPIO22_FL_STROBE_TRIG	Camera flash strobe trigger / Configurable GPIO
33	USB_VBUS	See JT2 pin 25
34	GPIO8_CAM_ELDO2_EN	Camera standby output 2 / Configurable GPIO
35	USB_CC2	USB Type C port – CC2 pin
36	GPIO29_BLO_EN	Display 0 backlight enable / Configurable GPIO
37	USB_CC1	USB Type C port – OTG mode enable or CC1 pin
38	GPIO9_CAM2_RST_N	Camera 2 reset output / Configurable GPIO
39	RGB_BLUE	RGB LED high-side current source: blue
40	PMI8998_LPG_WLED	PMI8998 GPIO_05 light pulse generator (for backlight PWM) / Configurable GPIO
41	RGB_GREEN	RGB LED high-side current source: green
42	PMI8998_SPKR_AMP_EN2	PMI8998 GPIO_11 speaker AMP enable output / Configurable GPIO
43	RGB_RED	RGB LED high-side current source: red
44	PMI_CHARGE_STAT	Battery charge status / fault / interrupt output indicator.
45	GPIO123	Sensor interrupt input / Configurable GPIO
46	GPIO126_SDC2_CARD_DET_N	Secure Digital card detect input / Configurable GPIO
47	HAPT_OUT_N	Haptics H-bridge driver output

Pin #	JT2 Signal Name	Description
48	GPIO21_FLASH_FRONT_EN	Camera flash enable / Configurable GPIO
49	HAPT_OUT_P	Haptics H-bridge driver output
50	GPIO10_LCD_TE0	Display vertical sync / Configurable GPIO
51	GPIO31_USB_VBUS_EN	USB Type A port VBUS output enable / Configurable GPIO
52	GPIO122_HRM_INT	Sensor interrupt input / Configurable GPIO
53	GPIO6_LCD_RST_N	Display 0 reset output / Configurable GPIO
54	GPIO32_TS1_RESET_N	Display 0 touchscreen reset output / Configurable GPIO
55	GPIO80_CAM0_RST_N	Camera 0 reset output / Configurable GPIO
56	GPIO79_CAM_ELDO9_EN	Camera standby output 9 / Configurable GPIO
57	GPIO7_LCD1_RST_N	Display 1 reset output / Configurable GPIO
58	GPIO124	Sensor interrupt input / Configurable GPIO
59	GPIO100_BOOTCFG_2	Boot Configuration bit 2 (Fast Boot Select bit 1) input during power on sequence. Configurable GPIO at other times.
60	GND	Ground reference for the SOM.
61	GPIO99_TS_RESET_N	Boot Configuration bit 1 (Fast Boot Select bit 0) input during power on sequence. Display touchscreen reset output / Configurable GPIO at other times.
62	USB_SBU_P	USB Type C port – Sideband / DisplayPort auxiliary channel
63	GPIO57_FORCE_USB_BOOT	Force USB Boot input for factory programming during power on sequence. Configurable GPIO at other times.
64	USB_SBU_N	USB Type C port – Sideband / DisplayPort auxiliary channel
65	GPIO125_TS_INT_N	Display touchscreen interrupt input / Configurable GPIO
66	GND	Ground reference for the SOM.
67	GND	Ground reference for the SOM.
68	GPIO55_QUP10_0_I2C_SDA	General purpose I2C / Configurable GPIO
69	PCIE1_TX_C_P	PCIE Gen3 Port 1 – transmit data
70	GPIO56_QUP10_1_I2C_SCL	General purpose I2C / Configurable GPIO
71	PCIE1_TX_C_N	PCIE Gen3 Port 1 – transmit data
72	GPIO58_QUA_MI2S_SCK	Quaternary MI2S (4-bit) / Configurable GPIO
73	GND	Ground reference for the SOM.

Pin #	JT2 Signal Name	Description
74	GPIO59_QUA_MI2S_WS	Quaternary MI2S (4-bit) / Configurable GPIO
75	PCIE1_REFCLK_N	PCIE Gen3 Port 1 – reference clock
76	GPIO61_QUA_MI2S_DATA1	Quaternary MI2S (4-bit) / Configurable GPIO
77	PCIE1_REFCLK_P	PCIE Gen3 Port 1 – reference clock
78	GPIO60_QUA_MI2S_DATA0	Quaternary MI2S (4-bit) / Configurable GPIO
79	GND	Ground reference for the SOM.
80	GPIO62_QUA_MI2S_DATA2	Quaternary MI2S (4-bit) / Configurable GPIO
81	PCIE1_RX_N	PCIE Gen3 Port 1 – receive data
82	GPIO63_QUA_MI2S_DATA3	Quaternary MI2S (4-bit) / Configurable GPIO
83	PCIE1_RX_P	PCIE Gen3 Port 1 – receive data
84	GPIO67_CODEEC_SPI_CLK	WCD9340 Audio Codec SPI port / Primary MI2S (2 bit) / Configurable GPIO
85	GND	Ground reference for the SOM.
86	GPIO68_CODEEC_SPI_CS_N	WCD9340 Audio Codec SPI port / Primary MI2S (2 bit) / Configurable GPIO
87	GPIO4_QUP9_2_DBG_UART_TX	Debug UART / Configurable GPIO
88	GPIO65_CODEEC_SPI_MISO	WCD9340 Audio Codec SPI port / Primary MI2S (2 bit) / Configurable GPIO
89	GPIO5_QUP9_3_DBG_UART_RX	Debug UART / Configurable GPIO
90	GPIO66_CODEEC_SPI_MOSI	WCD9340 Audio Codec SPI port / Primary MI2S (2 bit) / Configurable GPIO
91	SSC7_QUP1_5_SPI1_CS2_N	Snapdragon sensor core SPI 1
92	GPIO64_CODEEC_RST_N	WCD9340 Audio Codec reset output / Primary MI2S (2 bit) / Configurable GPIO
93	SSC2_QUP1_0_SPI1_MISO	Snapdragon sensor core SPI 1
94	GPIO54_CODEEC_INT1_N	Audio codec interrupt input / Configurable GPIO
95	SSC3_QUP1_1_SPI1_MOSI	Snapdragon sensor core SPI 1
96	GPIO102_PCIE1_RST_N	PCIE Gen3 Port 1 – reset signal / Configurable GPIO
97	SSC4_QUP1_2_SPI1_CLK	Snapdragon sensor core SPI 1
98	GPIO103_PCIE1_CLKREQ_N	PCIE Gen3 Port 1 – reference clock request signal / Configurable GPIO
99	SSC6_QUP1_4_SPI1_CS1_N	Snapdragon sensor core SPI 1
100	GPIO104_PCIE1_WAKE_N	PCIE Gen3 Port 1 – wake signal / Configurable GPIO

Table 4 – B2B Connector JT3 Pin-outs

Pin #	JT3 Signal Name	Description
1	VREG_L13A_2P95	PM845 LDO 13A +1.8V power output from SOM. Used for SD card IO voltage on the carrier board.
2	VREG_L21A_2P95	PM845 LDO 21A +2.95V power output from SOM. Used for the SD card VCC on the carrier board. 800mA is expected to be available for carrier board usage.
3	LN_BB_CLK2_WCD	Clock output for WCD9340 Audio Codec on carrier board
4	VREG_L21A_2P95	See JT3 pin 2
5	PM845_CAM_ELDO1_EN	PM845 GPIO_12 Camera standby output 1 / Configurable GPIO
6	VREG_L21A_2P95	See JT3 pin 2
7	PM845_CAM_ELDO4_EN	PM845 GPIO_09 Camera standby output 4 / Configurable GPIO
8	GND	Ground reference for the SOM.
9	GPIO11_LCD_TE1	Display vertical sync / Configurable GPIO
10	MIPI_DSIO_LANE3_N	MIPI display serial interface 0 data
11	GPIO27_CAM_ELDO3_EN	Camera standby output 3 / Configurable GPIO
12	MIPI_DSIO_LANE3_P	MIPI display serial interface 0 data
13	GPIO87_QUP5_2_LCD_SPI_CLK	Display touchscreen SPI port / Configurable GPIO
14	GND	Ground reference for the SOM.
15	GPIO86_QUP5_1_LCD_SPI_MOSI	Display touchscreen SPI port / I2C / Configurable GPIO
16	MIPI_DSIO_LANE2_N	MIPI display serial interface 0 data
17	VREG_L19A_3P0	PM845 LDO 19A +3.0V power output from SOM. Used for sensor AVDD connections on the carrier board. 600mA is expected to be available for carrier board usage.
18	MIPI_DSIO_LANE2_P	MIPI display serial interface 0 data
19	GPIO85_QUP5_0_LCD_SPI_MISO	Display touchscreen SPI port / I2C / Configurable GPIO
20	GND	Ground reference for the SOM.
21	GPIO88_QUP5_3_LCD_SPI_CS_N	Display touchscreen SPI port / Configurable GPIO
22	MIPI_DSIO_CLK_P	MIPI display serial interface 0 clock
23	GND	Ground reference for the SOM.
24	MIPI_DSIO_CLK_N	MIPI display serial interface 0 clock
25	MIPI_DSI1_CLK_P	MIPI display serial interface 1 clock
26	GND	Ground reference for the SOM.
27	MIPI_DSI1_CLK_N	MIPI display serial interface 1 clock
28	MIPI_DSIO_LANE1_N	MIPI display serial interface 0 data

Pin #	JT3 Signal Name	Description
29	GND	Ground reference for the SOM.
30	MIPI_DSI0_LANE1_P	MIPI display serial interface 0 data
31	MIPI_DSI1_LANE2_N	MIPI display serial interface 1 data
32	GND	Ground reference for the SOM.
33	MIPI_DSI1_LANE2_P	MIPI display serial interface 1 data
34	MIPI_DSI0_LANE0_P	MIPI display serial interface 0 data
35	GND	Ground reference for the SOM.
36	MIPI_DSI0_LANE0_N	MIPI display serial interface 0 data
37	MIPI_DSI1_LANE3_N	MIPI display serial interface 1 data
38	GND	Ground reference for the SOM.
39	MIPI_DSI1_LANE3_P	MIPI display serial interface 1 data
40	GPIO41_QUP3_L0_I2C3_SDA	PCIE I2C port / Configurable GPIO
41	GND	Ground reference for the SOM.
42	GPIO42_QUP3_L1_I2C3_SCL	PCIE I2C port / Configurable GPIO
43	MIPI_DSI1_LANE1_N	MIPI display serial interface 1 data
44	CABC	Display PWM input for backlight brightness control
45	MIPI_DSI1_LANE1_P	MIPI display serial interface 1 data
46	VREG_L19A_3P0	See JT3 pin 17
47	GND	Ground reference for the SOM.
48	PM_VCOIN	Optional +3V rechargeable coin cell backup battery connection to SOM.
49	MIPI_DSI1_LANE0_N	MIPI display serial interface 1 data
50	VREG_L14A_1P8	PM845 LDO 14A +1.8V power output from SOM. Typically used for display IO voltage on the carrier board.
51	MIPI_DSI1_LANE0_P	MIPI display serial interface 1 data
52	VDISP_P_OUT	PMI8998 display positive bias SMPS regulated output.
53	GND	Ground reference for the SOM.
54	VDISP_M_OUT	PMI8998 display negative bias SMPS regulated output.
55	VREG_S3A_1P35	PM845 SMPS S3A +1.35V power output from SOM. Typically used for sub-regulation of camera DVDD power rails on the carrier board. While shared with SOM peripherals, it is expected that up to 1.2A is available for carrier board usage.
56	VREG_S3A_1P35	See JT3 pin 55
57	VREG_S3A_1P35	See JT3 pin 55
58	VREG_S3A_1P35	See JT3 pin 55
59	GND	Ground reference for the SOM.

Pin #	JT3 Signal Name	Description
60	GPIO28_CAM1_RST_N	Camera 1 reset output / Configurable GPIO
61	HAPT_PWM_IN	Haptics PWM control input to PMI8998 PMIC
62	GPIO72_CODEEC_SLIMBUS_DATA1	WCD9340 Audio Codec Slimbus / Speaker I2S / Configurable GPIO
63	GPIO2_QUPO_L2_SPI_CLK	QUPO SPI, UART / Configurable GPIO
64	GPIO70_CODEEC_SLIMBUS_CLK	WCD9340 Audio Codec Slimbus / Speaker I2S / Configurable GPIO
65	GPIO0_QUPO_LO_SPI_MISO	QUPO SPI, UART, I2C / Configurable GPIO
66	GPIO71_CODEEC_SLIMBUS_DATA0	WCD9340 Audio Codec Slimbus / Speaker I2S / Configurable GPIO
67	GPIO1_QUPO_L1_SPI_MOSI	QUPO SPI, UART, I2C / Configurable GPIO
68	GPIO69_SPARE	Speaker I2S / Configurable GPIO
69	GPIO3_QUPO_L3_SPI_CS_N	QUPO SPI, UART / Configurable GPIO
70	APQ_RESOUT_N	Processor reset output used for indicating power on sequence.
71	GND	Ground reference for the SOM.
72	FLASH_LED1	Camera flash output (max 300mA).
73	USB2_SS_RX_N	USB Type A port – SuperSpeed Receive Data
74	FLASH_LED2	Camera flash output (max 300mA).
75	USB2_SS_RX_P	USB Type A port – SuperSpeed Receive Data
76	VREG_WLED	Display backlight LED current supply output
77	GND	Ground reference for the SOM.
78	WLED_SINK3	Display backlight LED current supply sink
79	USB2_HS_D_N	USB Type A port – high speed data
80	WLED_SINK1	Display backlight LED current supply sink
81	USB2_HS_D_P	USB Type A port – high speed data
82	WLED_SINK2	Display backlight LED current supply sink
83	GND	Ground reference for the SOM.
84	GND	Ground reference for the SOM.
85	USB2_SS_TX_C_P	USB Type A port – SuperSpeed Transmit Data
86	USB3_HS_D_P	USB Type C port – high speed data
87	USB2_SS_TX_C_N	USB Type A port – SuperSpeed Transmit Data
88	USB3_HS_D_N	USB Type C port – high speed data
89	GND	Ground reference for the SOM.
90	GND	Ground reference for the SOM.
91	USB3_SS_TX1_C_N	USB Type C port – SuperSpeed Transmit Data 1
92	USB3_SS_RX0_N	USB Type C port – SuperSpeed Receive Data 0

Pin #	JT3 Signal Name	Description
93	USB3_SS_TX1_C_P	USB Type C port – SuperSpeed Transmit Data 1
94	USB3_SS_RX0_P	USB Type C port – SuperSpeed Receive Data 0
95	GND	Ground reference for the SOM.
96	GND	Ground reference for the SOM.
97	USB3_SS_RX1_P	USB Type C port – SuperSpeed Receive Data 1
98	USB3_SS_TX0_C_N	USB Type C port – SuperSpeed Transmit Data 0
99	USB3_SS_RX1_N	USB Type C port – SuperSpeed Receive Data 1
100	USB3_SS_TX0_C_P	USB Type C port – SuperSpeed Transmit Data 0

4.3 RF Antenna Connections

The Open-Q 845 μ SOM provides WiFi and Bluetooth connectivity via the Qualcomm WCN3990 chipset. This provides 802.11 a/b/g/n/ac 2x2 MIMO, dual-band Wi-Fi, and Bluetooth 5.x. The 2x2 MIMO Wi-Fi requires two antennas for maximum throughput and operates at both 2.4GHz and 5GHz. Bluetooth uses only one of the antennas (CH0) and only operates at 2.4GHz. To support full performance of the Wi-Fi and Bluetooth, two dual-band antennas are required. If only Bluetooth is used, it can be supported with one single-band 2.4GHz antenna connected to the CH0 port.

The SOM uses two U.FL coaxial connectors (Hirose U.FL-R-SMT-1 (10)) for the antenna ports, as shown in the figure below.

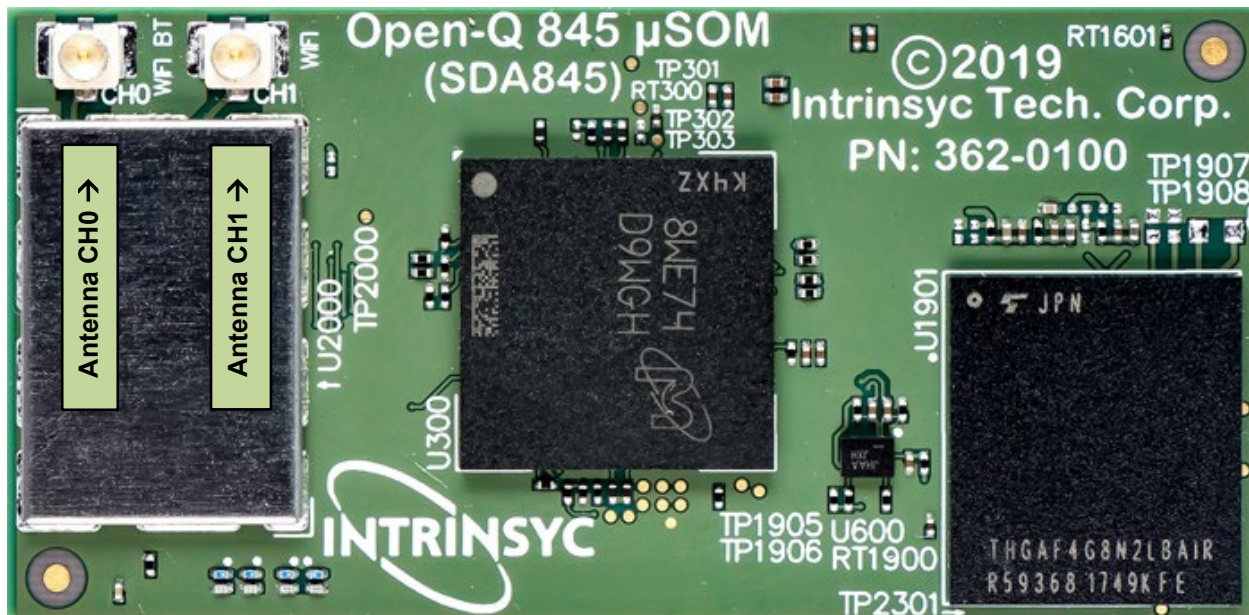


Figure 5 – Antenna Connection Locations on SOM

Table 5 – RF Signals via U.FL Coaxial Receptacles

Antenna	Description	Notes
Antenna CH0	RF chain 0 interface to Qualcomm WCN3990 chipset for Wi-Fi/BT	Antenna port for Wi-Fi and Bluetooth
Antenna CH1	RF chain 1 interface to Qualcomm WCN3990 chipset for Wi-Fi	Second antenna port for Wi-Fi 2x2 MIMO

5. Electrical Specifications

The input power to the SOM is provided by a power supply (battery or wall adapter) and also a USB source, for battery charging purposes. All input power sources enter the PMI8998 power management IC on the SOM, which then distributes power (along with the PM845 and PM8005 PMICs) to other circuits on the SOM and connected carrier board via LDO and switching power supply outputs.

5.1 Absolute Maximum Ratings

The table below shows the absolute maximum ratings in which the SOM input power sources can be exposed to without experiencing functional failure.

Table 6 – Absolute Maximum Input Power Ratings

Parameter	Min	Max	Units
Battery or DC power input (SOM_SYS_PWR)	-0.3	6	V
USB VBUS battery charger input voltage source (USB_VBUS)	-0.3	28	V

5.2 Operating Conditions

The table below shows the recommended operating conditions for the SOM to meet all performance specifications (provided the absolute maximum ratings have never been exceeded).

Table 7 – Operating Input Power Ratings

Parameter	Min	Typ	Max	Units
Battery or DC power input (SOM_SYS_PWR)	3.45 ¹	3.8	4.75	V
USB VBUS battery charger input voltage source (USB_VBUS)	3.6	5	14	V
VCOIN Input		3.2		V

5.3 Operating Temperature

The SOM operating temperature ratings listed below are based only on the operating temperature grade of the SOM components. Users should consider the specific environmental conditions in which the final product is used in.

Table 8 – Input Power Ratings for Operational Use

Parameter	Min	Typ	Max	Units
Overall SOM (case temperature)	-25	+25	+85	°C

¹ The SOM may be configured to operate at lower input voltage levels but changes to bootloader or proprietary code are needed and this will require support from Lantronix. Lantronix's solutions and software engineering services can provide advice and support for specialty low voltage requirements. Please contact Lantronix sales: <http://www.lantronix.com/about-us/contact/>

5.4 Power Consumption

Power consumption tests have been done on the SOM under common operational modes. These results are outlined in the table below. All tests were executed at room temperature on the Open-Q 845 μ SOM Development Kit running Android 9. The power consumption numbers listed in the table below reflect only what the SOM consumes during each operating mode.

Table 9 – Power Consumption Ratings

Operational Modes	Description	Average	Peak
Boot	Power consumption during boot process	N/A	8.7W
Suspend (Wi-Fi Off)	SOM placed in standby (Wi-Fi Off, Display Off)	0.06W	N/A
Suspend (Wi-Fi On)	SOM placed in standby (Wi-Fi On, Display Off)	0.09W	N/A
Suspend (SVA running, Wi-Fi Off)	SOM placed in standby with Snapdragon Voice Activation (SVA) running (Wi-Fi Off, Display Off)	0.06W	N/A
Idle (Display On)	SOM is idle (Wi-Fi Off, Display On)	0.74W	1.3W
Idle (Display Off)	SOM is idle (Wi-Fi Off, Display Off)	0.73W	1.3W
Video Record (1080P)	SOM recording 1080p video (Wi-Fi Off, Display On)	1.9W	4.3W
Video Record (4K UHD)	SOM recording 4K UHD video (Wi-Fi Off, Display On)	2.5W	5.5W
Video Playback (1080P)	SOM playing back 1080p video (Wi-Fi Off, Display On)	0.99W	1.8W
Video Playback (4K UHD)	SOM playing back 4K UHD video (Wi-Fi Off, Display On)	1.2W	3.5W
Audio Playback	SOM playing back MP3 audio file (Wi-Fi Off, Display Off)	0.79W	2.0W
Wi-Fi Download	SOM downloading data via Wi-Fi (Display Off)	3.1W	4.6W
Wi-Fi Upload	SOM uploading data via Wi-Fi (Display Off)	4.0W	6.8W
Full Load (All Cores)	SOM running all CPU cores (Wi-Fi Off, Display Off)	5.1W	6.9W
Single Core	SOM running single core (Wi-Fi Off, Display Off)	0.81W	1.6W
Bluetooth	SOM playing music over Bluetooth (Wi-Fi Off, Display Off)	0.81W	2.1W

5.5 ESD Ratings

The SOM is not designed with additional ESD protection other than what is included in the integrated circuits. It is recommended to take proper precautions in a static free environment when handling the SOM.

6. Mechanical Specifications

The sections below present some mechanical details of the Open-Q 845 μ SOM. For access to the 3D design files, please see <http://www.lantronix.com/products> (dev kit registration required).

6.1 SOM Mechanical Outline

The outer dimensions of the SOM are 50.0 x 25.0mm, as shown below.

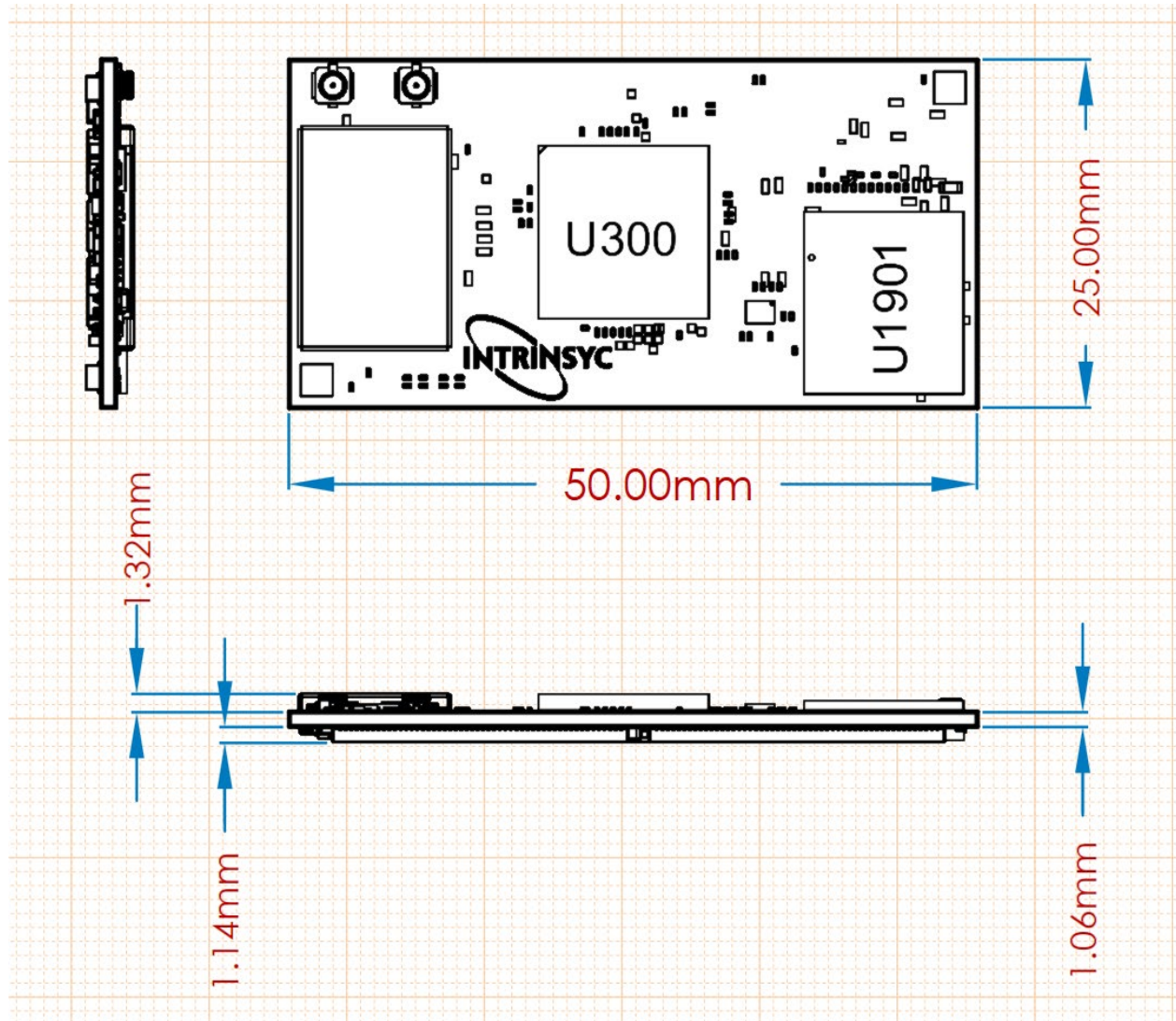


Figure 6 - SOM Mechanical Outline

6.2 Top and Bottom Height Restrictions

The tallest component on the top-side of the SOM is the WIFI shield at 1.32mm (nominal, see figure above). Please note that when the mating coax cables are connected, the top side height may be higher.

The tallest component on the bottom-side of the SOM is the board to board connectors at 1.14mm (nominal, see figure above).

6.3 Landing Pattern

Dimensions presented are in millimeters (mm). The footprint information in this section can be used as a guide when designing a landing area for the SOM.

Dimensions show the relative position of each connector on the SOM; referenced to the center of the connector body. NOTE: This information is given for reference. Please see SOM Carrier Board Design Guide for more detail (Reference document R-2).

*The perspective of this figure is looking through the top side of the SOM.

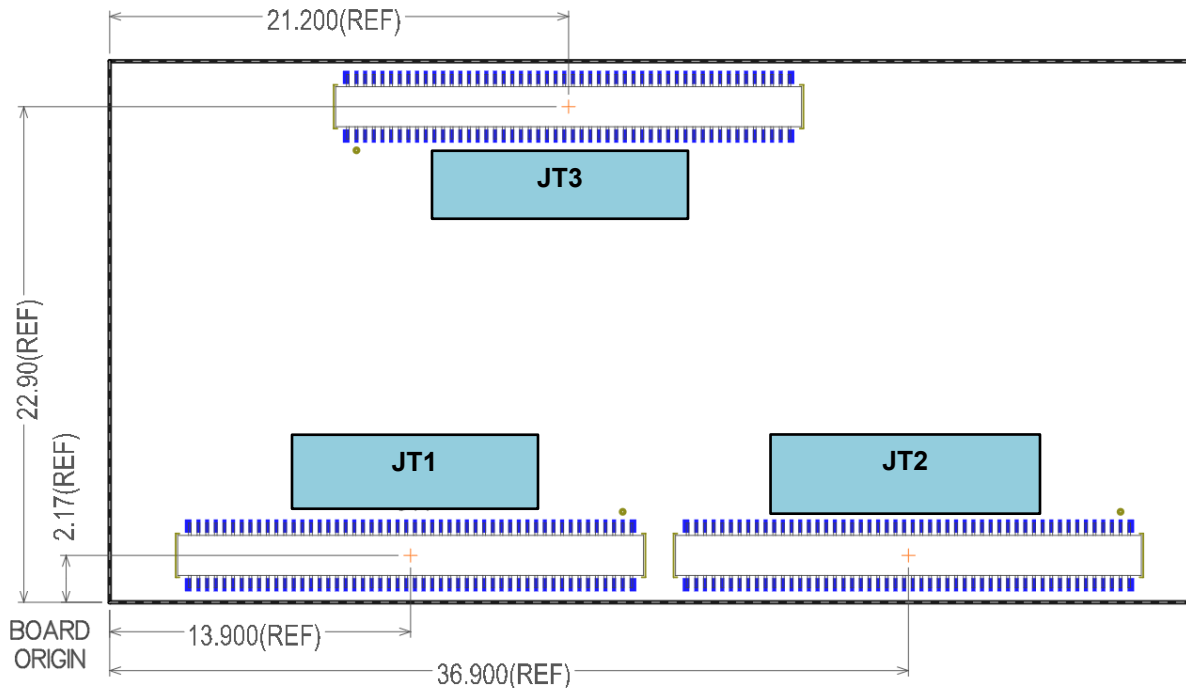


Figure 7 - SOM Land-Pattern Dimensions (mm)

The mating connector, Hirose DF40X-X-100DS-0.4V, is available in different heights, to achieve stack heights of 1.5mm or 3.0mm.

6.4 Thermal Characteristics

The SDA845 has built in thermal protections which will reduce processor frequency as the die temperature approaches set operating limits. These limits protect the processor from damage that could be caused by elevated die temperature. Additional product-level thermal management will remove heat from the SOM and its components, allowing the processor to run at higher frequencies for longer time periods before approaching the built in die temperature limits. This enables the average processor speed to remain higher through processor-intensive applications. Effectively removing heat from the Open-Q 845 μ SOM is required to optimize system performance and efficiency and to ensure that the SDA845 processor can perform as desired.

For more information on thermal mitigation, see SOM Carrier Board Design Guide (Reference document R-2).

6.5 Weight

The SOM weighs approximately 6 grams.

7. Product Marking, Ordering, and Shipping Info

7.1 Product Marking

The SOM part number and product marking can be identified on the white label on the top of the module. The figure and table below show a label example which includes the SOM name and QR code.



Figure 8 – Open-Q 845 μ SOM Label (top of PCB)

Table 10 – Open-Q 845 μ SOM Label Marking

Line	Marking	Description/ Notes
1	Open-Q 845 μ SOM	Lantronix product name
2	QR code *	<p>Embeds serial number and Wi-Fi MAC address. The serial number format is VVV-WWXX-YYYYYY-ZZZZZ</p> <ul style="list-style-type: none"> - VVV = Product number - WW = PCB revision number - XX = BOM revision number - YYYYYY = Date of manufacture (mm/dd/yy) - ZZZZZ = Unique serial number for PCB <p>The MAC address format is 0123456789AB</p> <ul style="list-style-type: none"> - 12 hexadecimal digit MAC address
<p>* QR code reader mobile app (e.g. Neo Reader) can be used to read embedded serial number and the MAC address.</p>		

7.2 Product Ordering Information

When available, the Open-Q 845 μ SOM can be ordered for evaluation and prototype use from Lantronix. For volume production orders or for custom requirements please contact sales at <http://www.lantronix.com/about-us/contact/>.

Orderable Part Numbers	
Open-Q 845 μ SOM std memory (32GB UFS + 4GB DDR)	QC-DB-P10004
Open-Q 845 μ SOM large memory (64GB UFS + 6GB DDR)	QC-DB-P10004B
Open-Q 845 μ SOM Development Kit	QC-DB-P10003

7.3 Packaging and Shipping Information

The Open-Q 845 μ SOM is packaged individually in small anti-static bags and bubble-wrap bags for protection during shipping – see Figure 9 below. They are then put into different sized boxes depending upon the quantity of the order. Small quantities are shipped in standard courier boxes with bubble-wrap protection and large quantity orders are packaged in a carton with dividers, as shown in Figure 10, below.



Figure 9 - Individual SOM Packaging



Figure 10 - Packaging for Large Quantity Shipments

8. Handling Precautions

8.1 ESD Precautions

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

The Open-Q 845 μ SOM is designed as a component meant to be integrated into a final product and therefore has no additional ESD protection built-in. It should be handled only in a static-safe environment to prevent damage.

8.2 SOM – Carrier Board Mating Cautions

Caution must be taken when connecting or disconnecting the SOM to a carrier board to prevent damage. Ensure that the SOM is inserted and removed straight up and down to prevent any sideways force on the connectors which could damage them.

Also note that the DF40C-100DX board to board connectors are rated for a maximum of 30 mating / unmating cycles. Therefore the number of insertions and removals must be limited to ensure reliability of the connectors.

8.3 Storage Conditions

The SOM must be stored in an antistatic bag.

Recommended Storage Conditions	
Temperature	-40 -> +85 °C
Humidity (non-condensing, relative)	5% -> 85 %

9. Certification

9.1 Radio Certification

The Lantronix Open-Q 845 μ SOM is expected to be certified with FCC and Industry Canada as a modular radio transmitter for WLAN and Bluetooth. When certification is complete, the FCC and Industry Canada ID numbers will be listed here.

9.2 ROHS/REACH Compliance

The Lantronix Open-Q 845 μ SOM is expected to comply with the ROHS/REACH standard. When compliance is complete, information on the ROHS/REACH certificate will be listed here.