



# Open-Q™ 820 Development Kit for Qualcomm™ APQ8096 Processor User Guide

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## Revision History

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December 2015	1.0	Initial release. Intrinsyc document number: ITC-01IMP1200-UG-001
January 2016	1.1	Second draft ready for release
February 2016	1.2	Third draft ready for release
April 2016	1.3	Replaced PMI8994 with PMI8996
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August 2020	A	Initial Lantronix document. Added Lantronix document part number, Lantronix logo, branding, contact information, and links.

For the latest revision of this product document, please go to: <http://tech.intrinsyc.com>.

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# 1. Introduction

## 1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q™ 820 Development Kit based on the Qualcomm™ APQ8096 Processor

For more background information on this development kit, visit:

<https://www.lantronix.com/products/open-q-820-development-kit/>

## 1.2 Scope

This document will cover the following items on the Open-Q 820:

- Block Diagram and Overview
- Hardware Features
- Configuration
- SOM
- Carrier Board
- Display Board for LCD (Optional)

## 1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Open-Q 820 Development Kit.

## 2. Documents

This section lists the supplementary documents for the Open-Q 820 development kit.

### 2.1 Applicable Documents

Reference	Title
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

### 2.2 Reference Documents

Reference	Title
R-1	Hardware Document Set for the Qualcomm APQ8096 based Open-Q Development Kit
R-2	Open-Q 820 Schematics (SOM, Carrier)
R-3	Open-Q 820 Dev Kit SOM Tech Note 13
R-4	ITCNFA324 Module Certification OEM Integrator Instructions

### 2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission

Term and acronyms	Definition
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SOM	System On Module
SPMI	System Power Management Interface (Qualcomm PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed



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## 3. Open-Q™ 820 Development Kit

### 3.1 Introduction

The Open-Q 820 provides a quick reference or evaluation platform for Qualcomm's latest 820 series - Qualcomm APQ8096 processor. This kit is suited for Android / Linux application developers, OEMs, consumer manufacturers, hardware component vendors, video surveillance, robotics, camera vendors, and flash chip vendors to evaluate, optimize, test and deploy applications that can utilize the Qualcomm 820 series technology.

### 3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at <http://www.fcc.gov/oet/rfsafety/>

### 3.3 Anti-Static Handling Procedures

The Open-Q 820 Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

### 3.4 Kit Contents

The Open-Q 820 Development Kit includes the following:

- Open-Q™ 820 SOM with the Qualcomm APQ8096 processor or main CPU board
- Mini-ITX form-factor carrier board
- 4.5" FWVGA (480x854) 16.7 M LCD (Additional Accessory)
- AC power adapter and HDMI cable



**Figure 1 Assembled Open-Q 820 Development Kit**

The development kit comes with Android 6.0 (Marshmallow) software pre-programmed on the CPU board (SOM). Please contact Lantronix for availability of camera modules, sensor boards, and other accessories: [sales@lantronix.com](mailto:sales@lantronix.com)

### 3.5 Hardware Identification Label

Labels are present on the CPU board and the mini-ITX form-factor carrier board. The following information is conveyed on these two boards:

CPU board:

- Serial Number
- WIFI MAC address [optional]

Refer to <https://tech.intrinsyc.com/projects/serialnumber/wiki> for more details about locating the serial number, as this will be needed to register the development kit. To register a development kit, please visit: <https://tech.intrinsyc.com/account/register>.

Mini-ITX form-factor carrier board:

- Serial Number

**Note:** Please retain the SOM and carrier board serial number for warranty purposes.

### 3.6 System Block Diagram

The Open-Q 820 development platform consists of three major components

- Open-Q 820 SOM
- Carrier board for I/O and connecting with external peripherals
- Display Adapter Board (additional accessory)

The following diagram explains the interconnectivity and peripherals on the development kit.

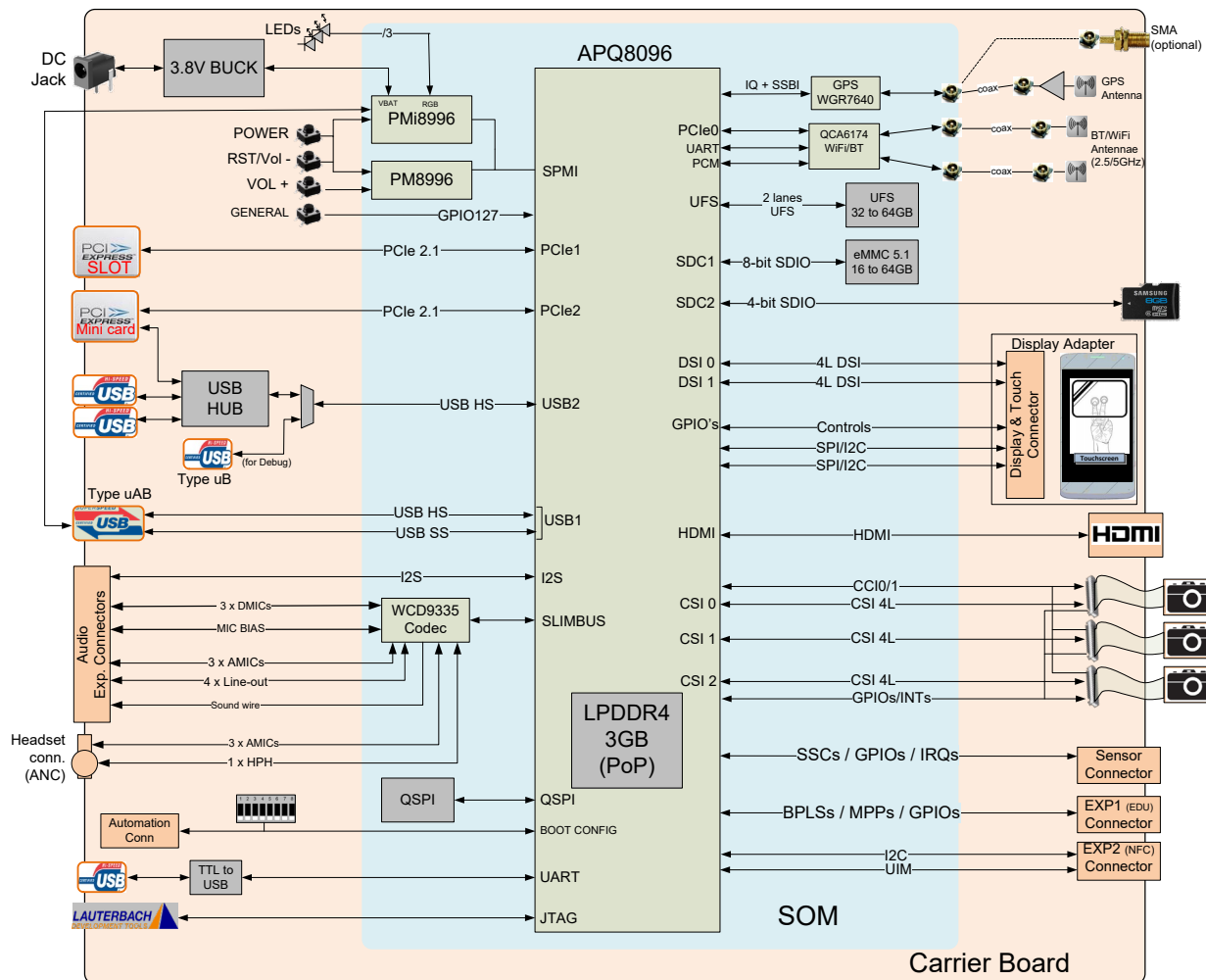


Figure 2 Open-Q 820 Block Diagram

### 3.7 Open-Q 820 SOM

The SOM provides the basic common set of features with minimal integration efforts for end users.

It contains the following:

- Qualcomm APQ8096 main application processor
- LPDDR4 up to 1866MHz 3GB RAM (POP)
- PMi8996 + PM8996 – PMIC for Peripheral LDOs, Boost Regulators

- QCA6174 Atheros Wi-Fi + BT combo chip over PCIe, UART, PCM
- 32 GB UFS 2.0.
- WGR7640 RF Front End
- WCD9335 Audio Codec

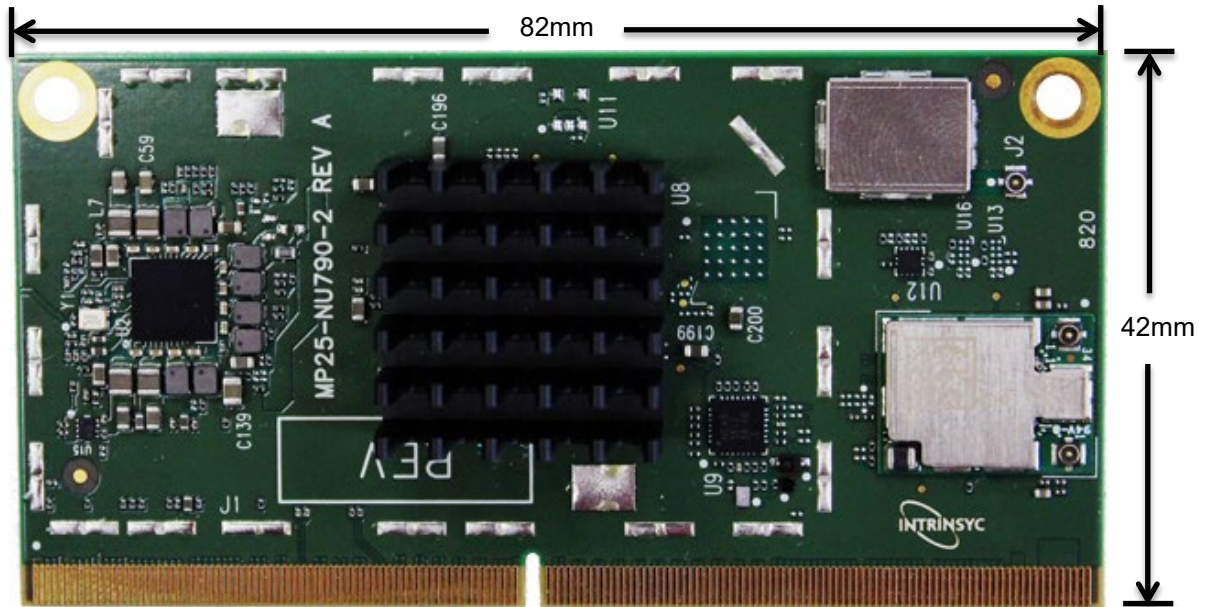


Figure 3 Open-Q 820 SOM

### 3.7.1 SOM Mechanical Properties

Area	34.44 cm <sup>2</sup> (42 mm x 82 mm)
Interface	314-pins MXM Gen-III edge connector & 100-pins SOM to carrier board connector (B2B Connector).
Thermal	A top side heat sink is installed by default.
Shielding	A top side shield can for the GPS front end is installed by default.

### 3.7.2 SOM Block Diagram

The Open-Q 820 SOM measuring 42mm x 82mm is where all the processing occurs. It is connected to the carrier via a 314-pin MXM Gen-III edge connector. The purpose of this edge connector is to bring out essential signals such that other peripherals can interface with the platform.

The SOM requires a board-to-board connector in addition to the MXM Gen III connector. This connector is responsible for bringing out the audio signals to the carrier board whereas the MXM connector exposes all other pin features supported by the SOC.

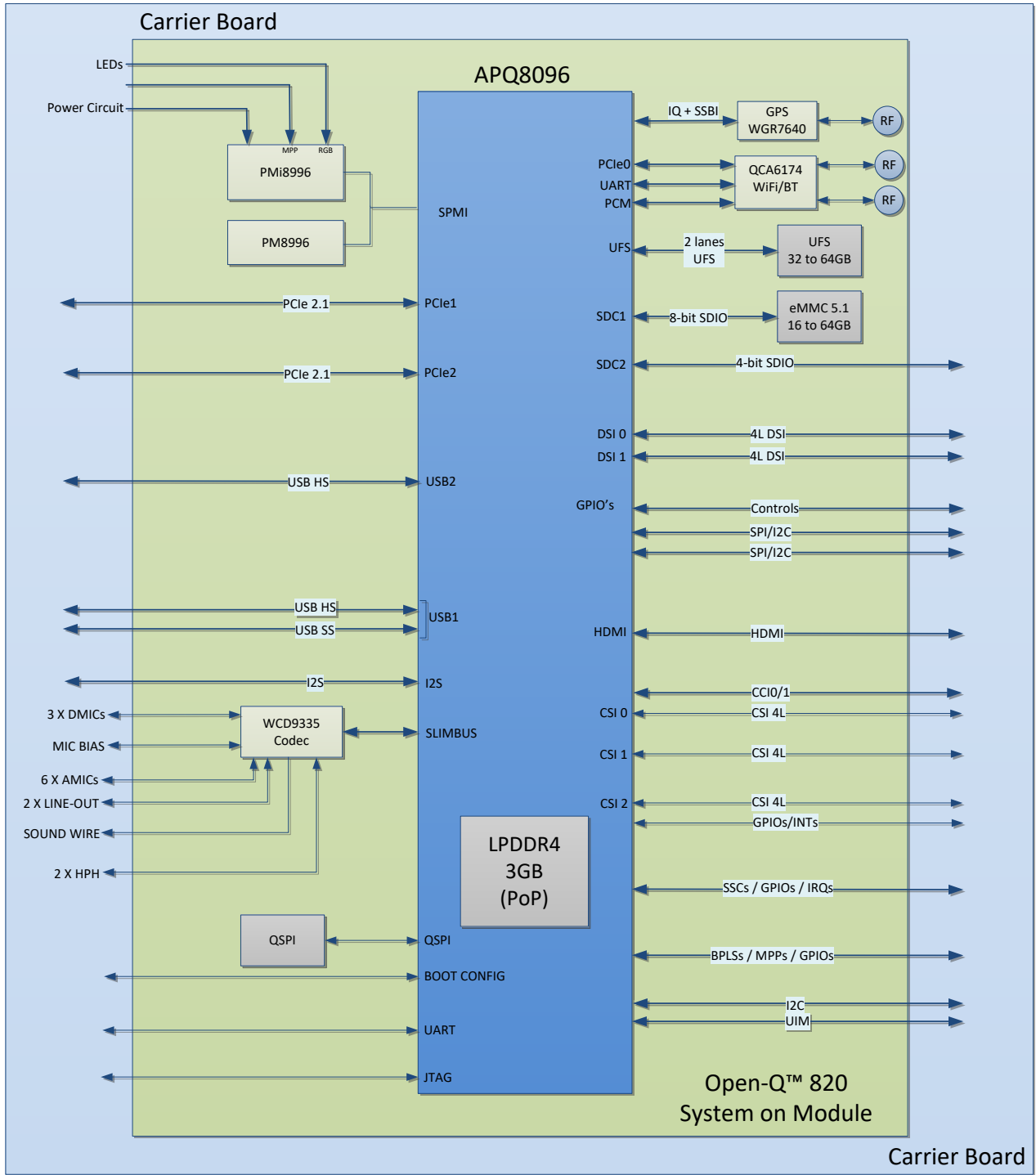


Figure 4 SOM Block Diagram

### 3.7.3 Hardware Specification

The Open-Q™ 820 SOM platform encompasses the following hardware features:

**Table 3.7-1 Open-Q Hardware Features**

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	APQ8096	Qualcomm® APQ8096 Processor	Qualcomm® Kyro CPU, quad core, 64-bit ARM V8 compliant processor, 2.2GHz
	PMIC (PM8996 & PMi8996)	Qualcomm® PMIC, Companion PMIC for APQ8096 processor	NA
Memory	3GB LPDDR4	Memory POP	Up to 1866MHz LPDDR4 POP on CPU BGA chip. Supports via 4x16bit channels
	32 GB UFS	Primary Storage for platform. Mainly used for storing SW applications and user data etc.	Toshiba UFS on board. Can support up to 64GB. Can have the option of using both UFS and eMMC.
Connectivity	Wi-Fi 2.4 GHz/ 5GHz via QCA6174 – SDIO	Wi-Fi Atheros QCA6174 Wi-Fi + BT Combo Chip	802.11a/b/g/n/ac 2.4/5.0 GHz via QCA6174 over PCIe0.  Full 2x2 antenna configuration
	BT 2.4 GHz via QCA6174 – UART / PCM	Wi-Fi Atheros 6174 Wi-Fi + BT Combo Chip	Support BT 4.1 + HS and backward compatible with BT 1.x, 2.x + EDR
	GPS via WGR7640 – SSBI Qualcomm Proprietary Protocol	GPS Frontend	GPS/ GLONASS/ COMPASS
RF Interfaces	2xWLAN / BT	Connect to antenna on carrier board via coax cable	2.4/ 5 GHz
	1x GPS	Connect to antenna on carrier board via coax cable	GPS/ GLONASS/ COMPASS
Audio Interfaces	1 x Headset Output	Headset/ headphone output	Analog differential output
	2 x Loud-speaker	2 x loud-speaker output	Digital output
	1 x Earpiece output	Earpiece output	Analog differential output



Subsystem / Connectors	Feature Set	Description	Specification
	3 x analog MICs	Analog MIC input	Analog differential input
	3 x digital MICs	Digital MIC input	Digital input
Interfaces	3 x MIPI CSI	Camera Connectors CSI0, CSI1, CSI2	MIPI Alliance Specification v1.0
	2 x USB HS & 1 x USB SS	1 x dual stack type A USB2.0 via USB HUB for front USB (from USB1 line), 1 x micro AB USB 3.0 via switch (from USB1 line), 1 x micro B USB 2.0 (from USB2 line)	USB3.1 & USB2.0
	1 x MIPI DSI (DSI0 & DSI1) + Touch 100-pin display Connector	100- pin display connector. Interfaces with Intrinysc Display Adapter Board	MIPI Alliance Specification v1.01. MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01
	3 X PCIe	PCIe 0 PCIe signal to Wi-Fi module. PCIe 1, 2 routed out of SOM	PCI Express Specification, Rev 2.1
Connectors	1 x MXM SOM connector	Connector for SOM	314 pin edge connector
	1 x SOM to Carrier board to board connector	B2B connector for SOM and carrier board	100 pin board to board connector

### 3.7.4 SOM RF Specification for WIFI, BT, GPS

The SOM includes the following radio interfaces:

- ANT1: Wi-Fi antenna 1 + BT
- ANT2: Wi-Fi antenna 2
- WGR7640: For GPS RF Front end

**Antenna 1:** The antenna 1 connector is for one of the two Wi-Fi antennas as well as the single Bluetooth antenna. Antenna connector ANT1 is connected to the carrier board antenna via a coaxial cable.

**Antenna 2:** The antenna 2 connector is for the second Wi-Fi antenna. This antenna connector is also connected to a carrier board PCB antenna via a coaxial cable.

Note that two dual-band (2.4GHz + 5GHz) antennas are required to be connected to achieve full performance of the Wi-Fi interface. If only Bluetooth is being used, then only a single 2.4GHz antenna connected to ANT1 is necessary.

The SOM WiFi/BT module has received regulatory certifications (see FCC ID: 2AFDI-ITCNFA324 for details). Please note that the on board PCB antennas were not the antennas used for the SOM WiFi/BT module certification. Refer to the certification documents for the WiFi/ BT module (see R-4) for information regarding the test configurations used for certification. Deviating from the documented configuration may trigger the need for re-certification.

For details on connecting the WiFi module to the on board PCB antennas on the carrier board, refer to section 3.8.14 below.

**WGR7640:** GPS Front End WGR7640 is the primary GPS radio interface used on the Open-Q 820 development kit. This provides the RF capabilities for GNSS functions.

The following are the operating frequencies for WGR7640

GPS: 1574.42 MHz – 1576.42 MHz

GLONASS: 1598 MHz to 1606 MHz

For more information about connecting a GPS antenna to the development kit see section 3.8.15 below.

## 3.8 Open-Q™ Carrier Board

The Open-Q 820 Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals. The following are the mechanical properties of the carrier board:

Dimensions	289 cm <sup>2</sup> (170mm x 170mm)
Form Factor	Mini-ITX
Major Interfaces	SOM: 314 pin FOXCONN connector SOM: 100 pin board to board connector Display: 100 pin carrier board connector
Thermal	Thermal pad is placed between the SOM and carrier board

### 3.8.1 Dip switch S10 Configuration Options

There is a DIP switch S10 on the top side of the Open-Q™ 820 carrier board. The 8-bit switch allows the user to control the system configuration and boot options. Table 3.8-1 below outlines the pin outs and connections of these DIP switches.

**Table 3.8-1 Dip Switch HW / SW Configuration**

Function	DIP Switch	Description	Notes
FORCED_USB_BOOT	S10-1	Toggles between FORCE USB boot and EDL mode. Enables FORCE USB (GPIO 57) when DIP switch turned on	Default out of the box configuration is OFF which is the EDL mode <b>Note:</b> FORCE USB boot option not supported by Lantronix
JTAG_PS_HOLD	S10-2	Enables the JTAG_PS_HOLD mode when DIP switch turned on	Default out of the box configuration is OFF <b>Note:</b> Lantronix does not provide software support for JTAG
BOOT_CONFIG[3]	S10-3	Enables APQ boot configuration 3 when DIP switch turned on. Controlled by APQ GPIO104  See schematic for boot configuration options.  NOTE: Some boot configurations are not supported on the development kit.	Default out of the box configuration is ON
BOOT_CONFIG[2]	S10-4	Enables APQ boot configuration 2 when DIP switch turned on. Controlled by APQ-GPIO103	Default out of the box configuration is OFF
BOOT_CONFIG[1]	S10-5	Enables APQ boot configuration 1 when DIP switch turned on. Controlled by APQ-GPIO 102	Default out of the box configuration is OFF

Function	DIP Switch	Description	Notes
WATCHDOG_DISABLE	S10-6	Enables WATCHDOG_DISABLE when DIP switch turned on. Controlled by APQ-GPIO 101	Default out of the box configuration is OFF
N/C	S10-7	NA	NA
GPS_ANT_SEL	S10-8	Option to select which antenna to use for GPS. When DIP switch ON GPS external antenna is being used (SMA connector). When switch OFF, GPS printed antenna is being used (on-board)	Default out of the box configuration is OFF

**Warning!:** Before making any changes to the dip switch, make sure to note down the previous configuration. The default switch settings are below.

### 3.8.2 Open-Q™ 820 Carrier Board Expansion Connectors

Table 3.8-2 lists the connectors, expansions and their usages on the carrier board:

**Table 3.8-2 Carrier Board Expansion Options and Their Usage**

Domain	Description	Specification	Usage
Power	AC / Barrel charger	12 V DC Power Supply 5 A	Power Supply
	Power connector	20 pin header	For providing extra current to camera connectors when needed (ie: when high performance cameras used)
Debug Serial via USB	Debug Serial UART console over USB for development	Vertical USB Micro B connector	Development Serial Connector for debug output via USB
JTAG	OS / Firmware /QFROM Programming / Debugging JTAG	Standard 20-pin connector, ARM and OpenDSP – Lauterbach	QFROM / eMMC / Platform EEPROM programming ARM / Open DSP debugging Note : JTAG is not supported
Buttons	General Purpose SW button	SMD Button	Additional button for general purpose
	Power Button	SMD Button	Power Button for Suspend / Resume and Power off
Volume Keys	Volume + key	SMD Button	Volume +Key

Domain	Description	Specification	Usage
	Volume – key	SMD Button	Volume – Key
Sensor IO Connector (DNP)	24 pin Sensor Expansion Connectors  Supports Gen-9 sensor connector as stuff option	Support any user sensor card,  Standard 44-pin ST Micro PLCC support via optional daughter card	Available via Lantronix optional accessories kit
NFC Board Header (EXP1)	20 pin NFC expansion connectors	NA	NA
GPIO / Education connector Header	16-pin general purpose IO for SPI / I2C / GPIOs/ UIM/ UART functions and other unused GPIOs from PMIC and APQ education header.	Full BLSP1 (SPI/ UART/ I2C/ GPIO)  APQ GPIOs  PMIC GPIOs  MPPs  GPLED sink  Power  Proprietary 16-pin header	Useful when user wants to use UART GPIOs pins as BLSP other functions (GPIO/ I2C/ UIM/ SPI).
Micro SD (on bottom)	Micro SD card	4bit Micro SD card support	External Storage
ANC Audio Jack	Audio Jack  Supported using WCD9335	ANC audio jack providing 2lineout and 1 headset drivers (shared with ANC)	Audio support
3-Digital Microphone via audio input expansion header	Audio expansion  Supported using WCD9335	Digital Audio header	For Digital audio input for Digital MIC, I2S codec, Slim bus interface.
3-Analog Microphone via audio input expansion header	Audio expansion  Supported using WCD9335	Analog Audio header	For Analog audio input for Analog MIC (differential signal)
2-Loud Speaker via audio output expansion header	Audio expansion  Supported using WCD9335	Analog Audio header	For loud speaker output after signal has been processed
Earpiece via audio output expansion header	Audio expansion  Supported using WCD9335	Analog Audio header	For earpiece output after signal has been processed
HDMI Port	Extended Display ports	HDMI port supports up to 4K without HDCP 1.4A spec	External Display
USB OTG	USB 2.0 OTG	Micro B connector	USB debugging and client / host mode
USB 3.0	USB 3.0	Micro AB header	Transfer data to and from

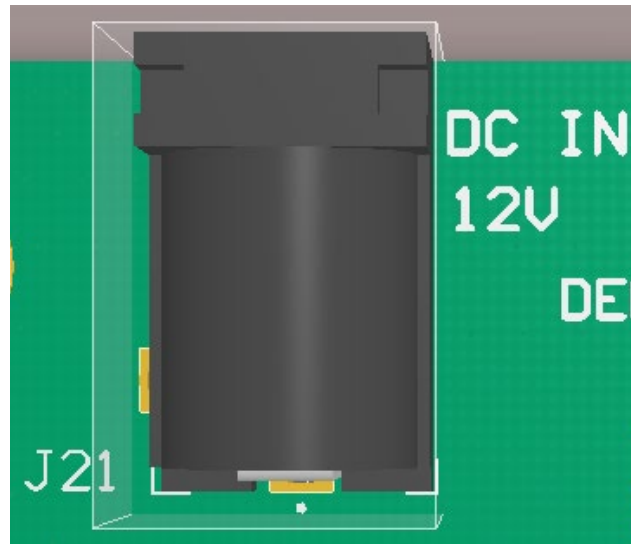
Domain	Description	Specification	Usage
			CPU
WLAN Antenna	2X PCB Antenna	2.4 – 5.1 GHz	Antenna to SOM WiFi module
GPS Antenna	PCB Antenna	GPS : 1574.42 MHz – 1576.42 MHz  GLONASS :  1587 MHz – 1606 MHz	Antenna to SOM GPS module
Coin Cell Holder(Optional)	Coin Cell battery(Optional via stuffing)	Coin cell battery for PMIC RTC	RTC
LED	3xLED	Red : PMIC Driven  Green: PMIC Driven  Blue: PMIC Driven	Blue : General purpose  Red : General purpose  Green : General purpose
LCD Display and Touch connector	100 pin for LCD signals from b2b boards for display	4-lane MIPI DSI0 , DSI1  I2C/SPI/GPIO  Backlight  MIPI Alliance Specification v1.01  MIPI D-PHY Specification v0.65,v0.81, v0.90, v1.01	Can work as one dual DSI or both independent display
Sensor header	24 pin sensor header	24 pin sensor header	Header to connect sensor board. Please contact Lantronix for availabilities of this board
Automation connector	Automation connector for continuous integration systems	20 pin header	For automating tests on the board by controlling the board to power on and off as well as SW download
Gen10 connector	Connector for Qualcomm's internal sensor boards	60 pin connector sensor Gen 10	To interface with Qualcomm's internal sensor boards <b>(for Lantronix internal use only – not supported)</b>
VIP Extension connector	Connector for interfacing with Qualcomm legacy automotive VIP boards	60-pin connector	To connect to Qualcomm legacy automotive VIP boards <b>(for Lantronix internal use only – not supported)</b>
Ethernet AVB connector	Connector for interfacing with Ethernet AVB standard	60-pin connector	To connect to automotive peripherals via Ethernet AVB standard <b>(for Lantronix internal use only – not supported)</b>

Domain	Description	Specification	Usage
			<b>supported)</b>
PCI Express Slot	PCI Express for external peripheral connectivity	PCIe1 v2.1  Supports half card only  Supports 10W card via power supply  Supports 25W card via ATX power supply	To connect an Ethernet PCIe card board to support Ethernet.
Mini PCI Express Connector	Mini PCI Express for external peripheral connectivity	PCIe1 v2.1  Can support half or full size card	For external mini PCIe card
WWAN SIM Card (on bottom)	WWAN SIM card connector (optional)	4bit Mini SIM card support	For WWAN mini PCI express cards
CSI Camera connectors	3 x CSI port connector with CLK, GPIOs, CCI	Supports 3 x Camera interfaces via three separate connectors  <ul style="list-style-type: none"> <li>• 3 x MIPI-CSI each 4 lane</li> <li>• External flash driver control</li> <li>• Support for 3D camera configuration</li> <li>• Separate I2C / CCI control</li> </ul> MIPI Alliance Specification v1.00 for Camera Serial Interface	For connecting camera accessories.
Power Probe Header	3 pin power probe header	Sense lines connected across 0.005 Ohm resistor	To measure current consumption of $\mu$ SOM

The following sections will provide in depth information on each expansion headers and connectors on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-Q™ 820. Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the processor.

### 3.8.3 Open-Q Power Specification

The Open-Q™ development kit power source connects to the 12V DC power supply jack J21. Starting from the power jack, the 12V power supply branches off into different voltage rails via step down converters on the carrier board and PMIC on the SOM. The SOM is powered by 3.8V via Richtek step down converter U2 on the carrier board. To ensure the SOM is getting powered correctly, user can monitor the current going into the SOM via the power probe header J86 (see section [below](#)).



**Figure 5 J21 12V DC Power Jack**

The SOM consists of 2 PMIC modules. Functionalities of the 2 modules are outlined below.

PMI8996 PMIC is used for:

- Source various regulated power rails
- Support for battery charging on the PMI8996 is not implemented on the platform. The carrier board uses a 3.8V constant power input to the SOM.
- Support for battery charging over external charger is not implemented in the design. Please contact Lantronix for such customization.

PM8996 PMIC is used for:

- Source various regulated power rails
- Source system clock

### 3.8.4 Power Probe Header J86



**Figure 6 J86 Power Probe Header**

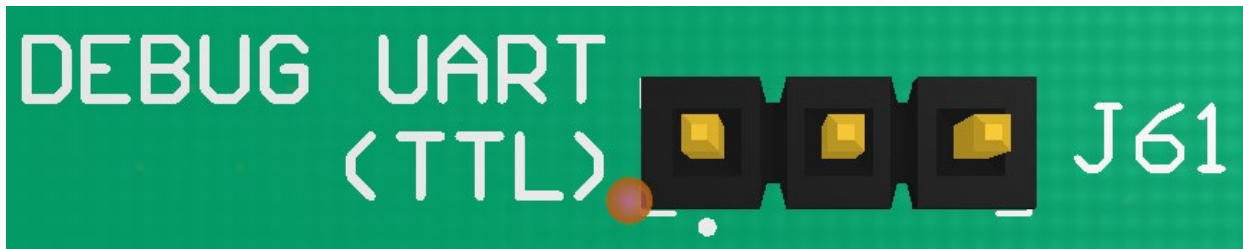
The power probe header is used to sense/ monitor the current on the 3.8V power rail going into the SOM. The table below summarizes the pin outs of header J86.



**Table 3.8-3 Power Header J86 Pin-out**

Description	Signal	pin
SOM power positive current sense line	SOM_PWR_SENSE_P	J86[1]
SOM power negative current sense line	SOM_PWR_SENSE_N	J86[2]
GND	GND	J86[3]

### 3.8.5 Debug Serial UART Header J61

**Figure 7 J61 3.3V TTL Debug UART**

The UART header and supporting circuitry does not come preinstalled. To have access to the debug UART, a 3-pin header needs to be installed as well as the supporting circuitry. Please see page 16 of the carrier board schematic for details on what to install for this header to be functional.

The header consists of TX, RX and GND pins. It is a 3.3V TTL UART header. To get the serial terminal working with a PC, the following cable (or similar) is needed

<http://www.digikey.ca/product-detail/en/TTL-232R-RPI/768-1204-ND/4382044>

**Table 3.8-4 Debug UART Header J61 Pin-out**

Description	Signal	pin	FTDI RPI cable connection
APQ UART RX (GPIO5)	BLSP8_UART_RX	J61[1]	Orange
APQ UART TX (GPIO4)	BLSP8_UART_TX	J61[2]	Yellow
GND	GND	J61[3]	Black

### 3.8.6 Debug Serial UART Over USB J22

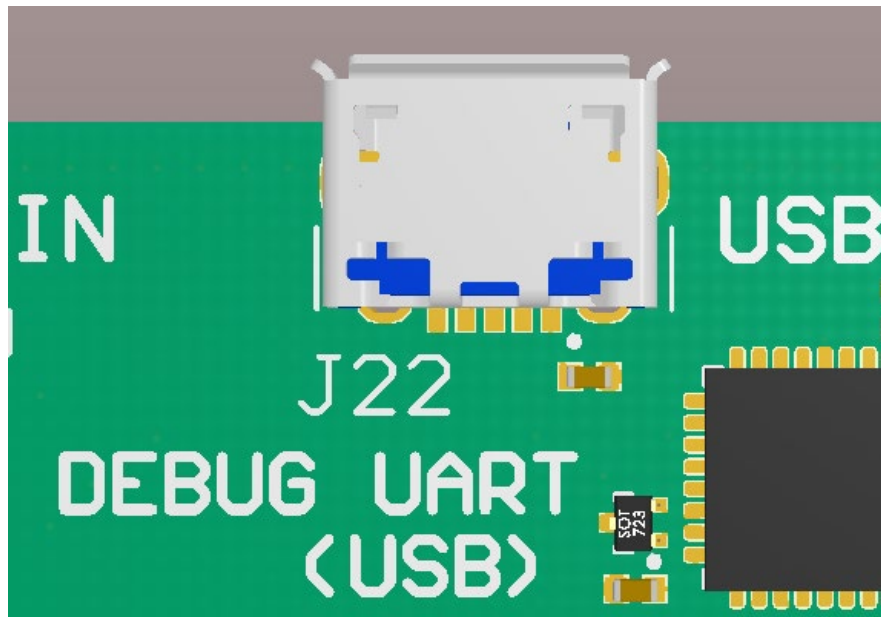


Figure 8 J22 Debug UART Over USB

The UART connection used on the Open-Q 820 is a USB micro B connector (J22). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed.

### 3.8.7 JTAG Header J51

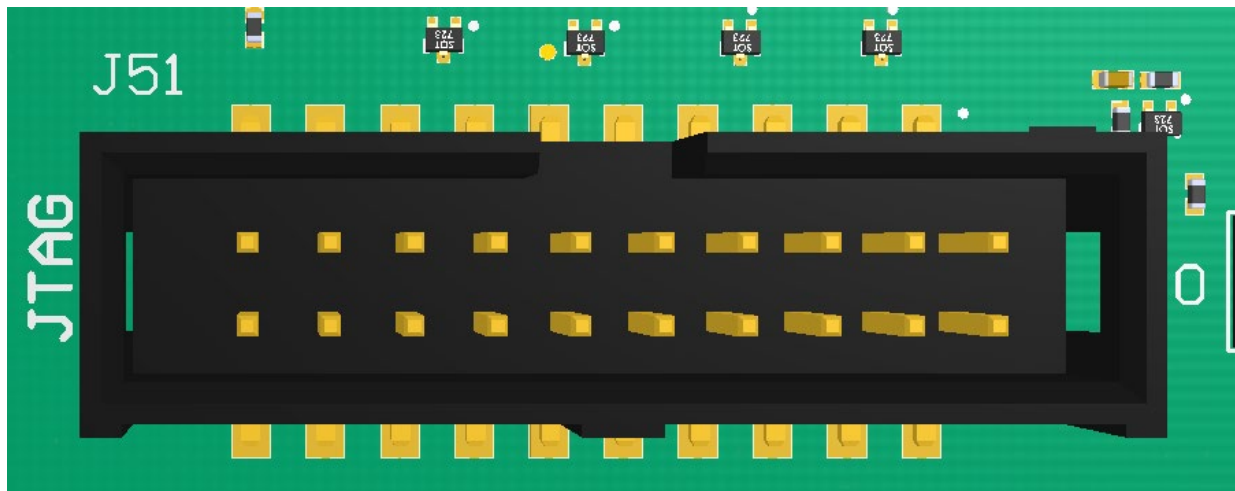


Figure 9 J51 JTAG Header

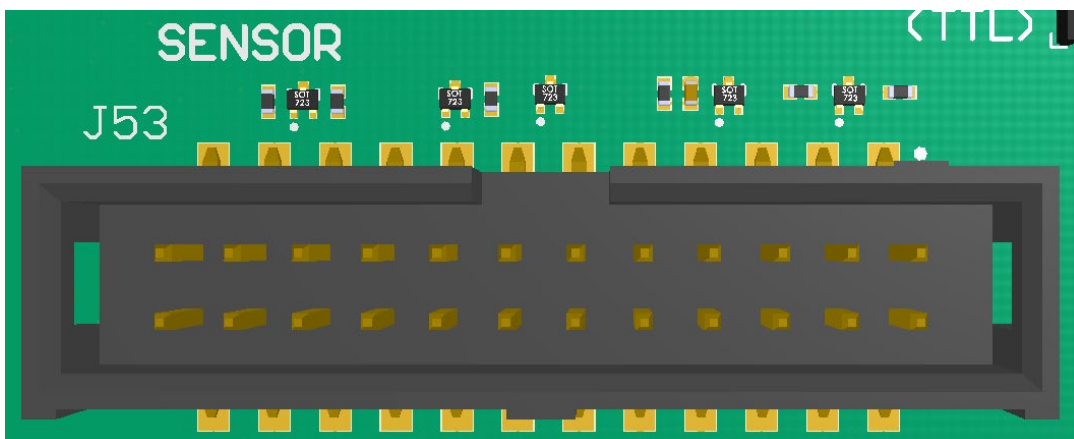
This connector provides a JTAG interface to the main processor by which users can connect a JTAG (Lauterbach / USB Wiggler) 20 pin ARM JTAG.

**Note:** Lantronix does not provide software support for JTAG

**Table 3.8-5 JTAG Header J51 Pin out**

Description	Signal	Pin NO	Description	Signal	Pin NO
GND	GND	J51[2]	JTAG Power detect	JTAG_PWR	J51[1]
GND	GND	J51[4]	Target RESET_N signal	TRST_N	J51[3]
GND	GND	J51[6]	TDI Signal (Target DATA IN)	TDI	J51[5]
GND	GND	J51[8]	TMS Signal	TMS	J51[7]
GND	GND	J51[10]	TCK Signal	TCK	J51[9]
GND	GND	J51[12]	JTAG_RTCK signal	JTAG_RTCK	J51[11]
GND	GND	J51[14]	TDO Signal (Target Data Out)	TDO	J51[13]
GND via 4.7KΩ pull down	GND	J51[16]	Source RESET_N signal	SRST_N	J51[15]
GND	GND	J51[18]	NC	NC	J51[17]
JTAG detect N signal	DET_N	J15[20]	GND via 4.7KΩ pull down	GND	J25[19]

### 3.8.8 Sensor IO Expansion Header J53



**Figure 10 J53 Sensor Expansion Header**

The sensor expansion header J53 allows for a 24-pin connection to an optional sensor board. If user application does not require a sensor, then this header can be used for other applications that require I2C or GPIO input and output connections.

Following is the pin breakout for sensor expansion header J53.

**Table 3.8-6 Sensor Expansion Header J53 Pin out**

Description	Signal	Pin NO	Description	Signal	Pin NO
SSC I2C-3 serial data	SSC_I2C_3_SDA	J53[1]	Accelerometer interrupt input to processor via GPIO117	ACCEL_INT_N	J53[2]
SSC I2C-3 serial clock	SSC_I2C_3_SCL	J53[3]	Cap interrupt input to processor via GPIO123	CAP_INT_N	J53[4]
Sensor reset signal from processor to sensor via GPIO80	MEMS_RESET_N	J53[5]	Gyroscope interrupt input to processor via GPIO118	GYRO_INT	J53[6]
Sensor IO PWR 1.8 V VREG_LVS2A_1P8 power supply regulator (Digital)	SENS_IO_PWR	J53[7]	Sensor Analog power supply from VREG_L19A 2.85V or 3.3V (If R160 populated)	SENS_ANA_PWR	J53[8]
GND	GND	J53[9]	GND	GND	J53[10]
HRM interrupt/ configurable GPIO122	HRM_INT	J53[11]	Touch screen interrupt input from processor via GPIO125	TS_INT0	J53[12]
SSC SPI-1 chip select 2	SSC_SPI_1_CS1_N	J53[13]	Alternate sensor interrupt input to processor via GPIO120	ALSPG_INT_N	J53[14]
MISC GPIO for sensor via GPIO84	APQ_GPIO84	J53[15]	Digital Compass interrupt input to processor via GPIO119	MAG_DRDY_INT	J53[16]
NC	NC	J53[17]	NC	NC	J53[18]
SSC SPI-1 chip select 1	SSC_SPI_1_CS_N	J53[19]	SSC SPI-1 data master out/ slave in	SSC_SPI_1_MOSI	J53[20]
SSC SOI-1 clock	SSC_SPI_1_CLK	J53[21]	SSC SPI-1 data master in/ slave out	SSC_SPI_1_MISO	J53[22]
NC	NC	J53[23]	SSC power enable	SSC_PWR_EN	J53[24]

In sum, if sensor application is not needed, this expansion header can provide two full BLSP7 and BLSP5 for UART/ SPI/ I2C/ UIM. Please refer to the schematic and consider the power before connecting anything to this header.

Note that there is an unpopulated Gen-10 connector header (J55) footprint at the bottom of the carrier board. Install the Samtec (part number: QSH-030-01-L-D-A) connector here if needed.

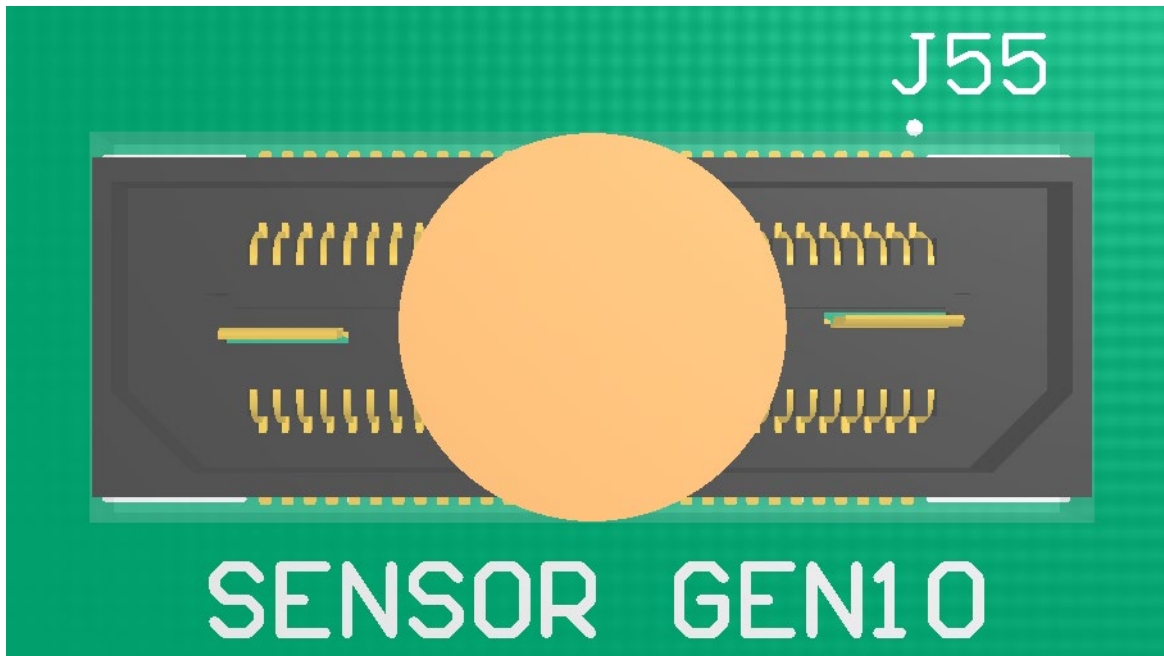


Figure 11 J55 Gen-10 Sensor Connector (Samtec QSH-030 series)

### 3.8.9 NFC Expansion Header J52 (EXP1)

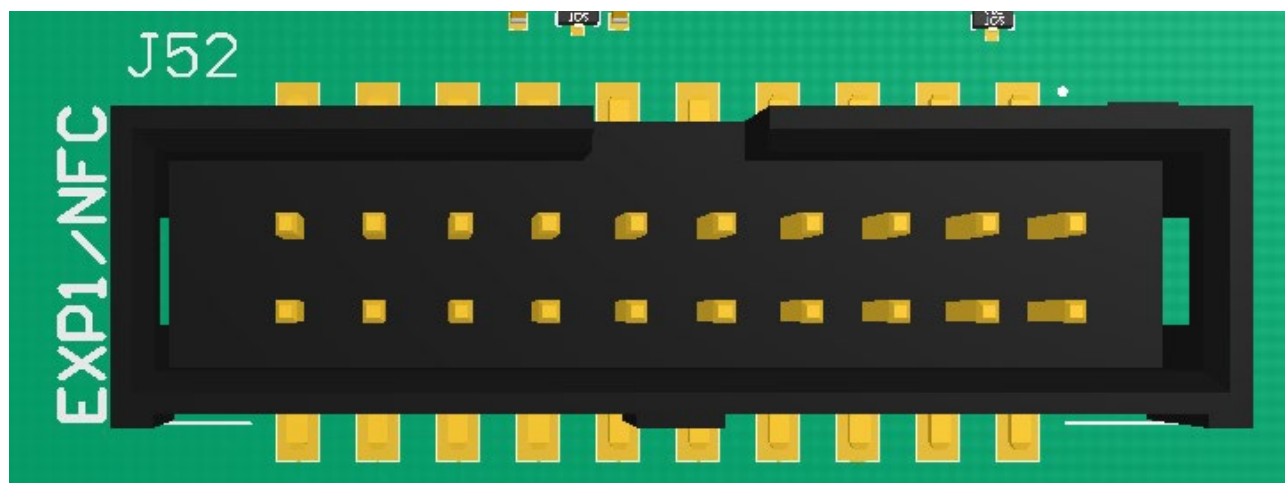


Figure 12 J52 NFC Expansion Header (EXP1)

The NFC expansion header provides a 20 pin connector for attaching an optional NFC board (please contact Lantronix for availability of the NFC board at [sales@lantronix.com](mailto:sales@lantronix.com) or visit <http://shop.intrinsyc.com>). This header also allows user to connect to the free GPIOs and I2C lines when NFC is not used; therefore, enabling

other use cases. Please refer to Table 3.8-7 for detailed information regarding the signals that are being brought out by this connector.

Note that this NFC expansion header is also compatible with the APQ8074 DragonBoard but the extra last four pins should not be connected.

**Table 3.8-7 NFC Expansion Header J52 Pin out**

Description	Signal	Pin NO	Description	Signal	Pin NO
BLSP9 bit 0 via APQ GPIO52	NFC_BLSP9_SP I_CLK	J52[1]	BLSP9 bit 2 via APQ GPIO50	NFC_BLSP9_SP I_MISO	J52[2]
NFC power request GPIO via PM GPIO7	NFC_PWR_REQ	J52[3]	SIM present GPIO via APQ GPIO112	UIM1_PRESENT	J52[4]
SIM Card DATA line (UIM1) via APQ GPIO109	UIM1_DATA	J52[5]	150mA max 3.8V SOM power supply pin	SOM_SYS_PWR	J52[6]
SIM Card Reset line (UIM1) via APQ GPIO111	UIM1_RESET	J52[7]	NFC interrupt IRQ pin via APQ GPIO106	NFC_IRQ	J52[8]
SIM CLK line (SIM1) via APQ GPIO110	UIM1_CLK	J52[9]	NFC Disable signal via APQ GPIO105	NFC_DISABLE	J52[10]
1.8V Voltage regulator supply max 150mA via PM8996	VREG_L9A_1P8	J52[11]	BLSP8 I2C Bus-8 I2C SDA line	BLSP8_I2C_SDA	J52[12]
1.8V Voltage regulator supply max 150mA via PM8996	VREG_S4A_1P8	J52[13]	BLSP68I2C Bus-8 I2C CLK line	BLSP8_I2C_SCL	J52[14]
GND	GND	J52[15]	NFC clock request signal via PM GPIO10	NFC_CLK_REQ	J52[16]
PM8996 free running clock via buffer	BBCLK2	J52[17]	SIM Card Reset line (UIM2) via APQ GPIO107	APQ_GPIO107	J52[18]
BLSP9 1 bit via APQ GPIO51	NFC_BLSP9_SP I_CS_N	J52[19]	BLSP9 3 bit via APQ GPIO49	NFC_BLSP9_SP I_MOSI	J52[20]

In general, if there is no need for NFC application, this expansion header can provide two GPIOs, I2C, free running clocks, and enable voltage/ power source to external peripherals.

### 3.8.10 Education / GPIO header J54 (EXP2)

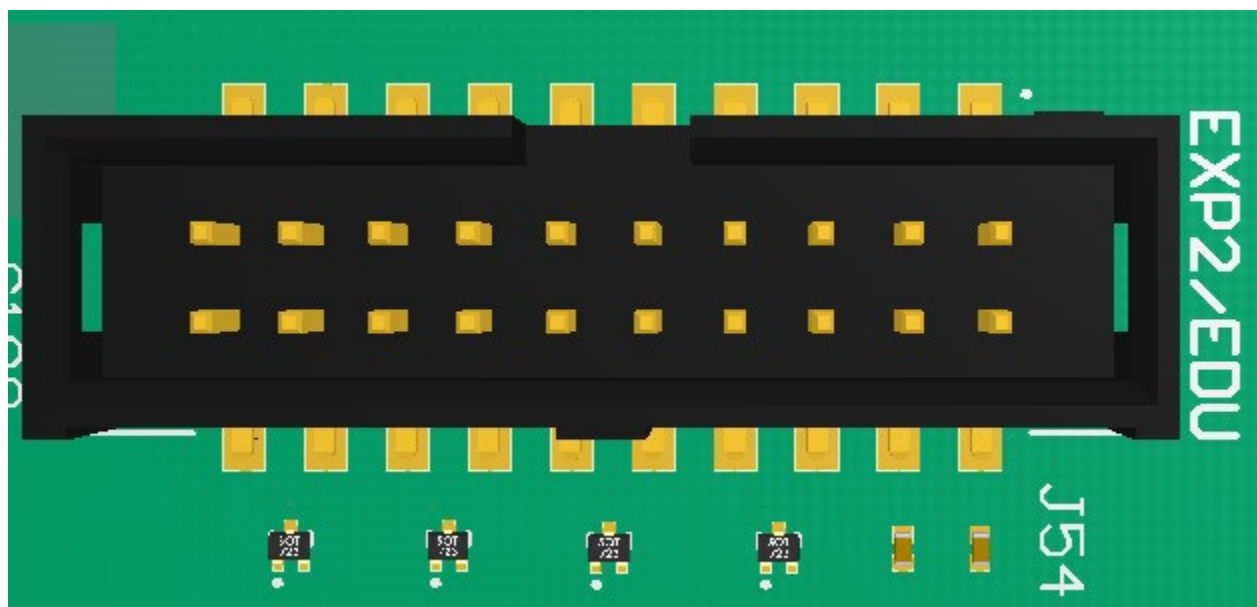


Figure 13 J54 Education / GPIO Header

Education/ GPIO header expansion J54 is a 20 pin connector that provides access to BLSP1 signals with level shifters. It is ideally used for connecting external peripherals such as microcontrollers and any other devices that are based on I2C, SPI, UART, UIM and GPIO. Please refer to the SOM schematic for the level shifter, target voltage and current rating depending on stuffing option. The education expander also supports multiple voltage ratings. The table below outlines the configurations for these settings:

Voltage Rails	Resistors to Populate (0 Ohm)
MB_VREG_3P3 – 3.3 V	R150 (Default)
VREG_S4A_1P8 – 1.8V	R149
MB_VREG_5P0 – 5.0 V	R151

The following are the detailed pin out information for education header J54.

Table 3.8-8 Education Connector Expansion Header J54 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
NC	NC	J54[1]	VREG_S4A 1.8V voltage regulator max 150mA	VREG_S4A_1P8	J54[2]
BLSP1_3_3P3(3.3V)	BLSP1_SPI_MOSI (APQ-GPIO0)	J54[3]	VDD_EXP2 (Default 3.3V Power Supply) max 300mA	VDD_EXP2	J54[4]

Description	Signal	Pin NO	Description	Signal	Pin NO
BLSP1_2_3P3(3.3V)	BLSP1_SPI_MISO (APQ-GPIO1)	J54[5]	PM8996 MPP GPIO2	PM_MPP02	J54[6]
BLSP1_1_3P3(3.3V)	BLSP1_SPI_CS_N (APQ-GPIO2)	J54[7]	PM8996 MPP GPIO4	PM_MPP04	J54[8]
BLSP1_0_3P3(3.3V)	BLSP1_SPI_CLK (APQ-GPIO3)	J54[9]	PM8996 MPP GPIO1	PM_MPP01	J54[10]
APQ-GPIO124 level shifted output / input (3.3V)	EXP_IRQ_3P3	J54[11]	PM8996 MPP GPIO6	PM_MPP06	J54[12]
APQ-GPIO84 level shifted output / input (3.3V)	APQ_GPIO84_3P3	J54[13]	APQ GPIO127 GPIO (3.3V) for general purpose input / output	APQ_GPIO127_3P3	J54[14]
PM8996 MPP GPIO03	PM_MPP03	J54[15]	PM8996 GPIO13 GPIO for general purpose input / output	PM_GPIO13	J54[16]
GND	GND	J54[17]	APQ GPIO134 GPIO (3.3V) for general purpose input / output	APQ_GPIO134_3P3	J54[18]
PM8996 DIVCLK3 via GPIO17	DIVCLK3_BUF	J54[19]	5V power supply max 150mA	MB_VREG_5P0	J54[20]

### 3.8.11 ANC Headset Jack J27

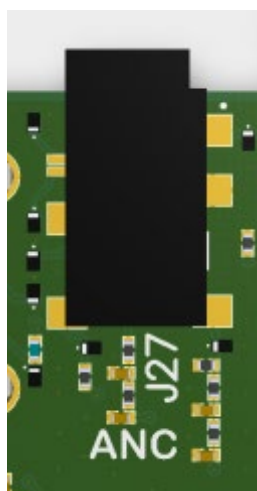
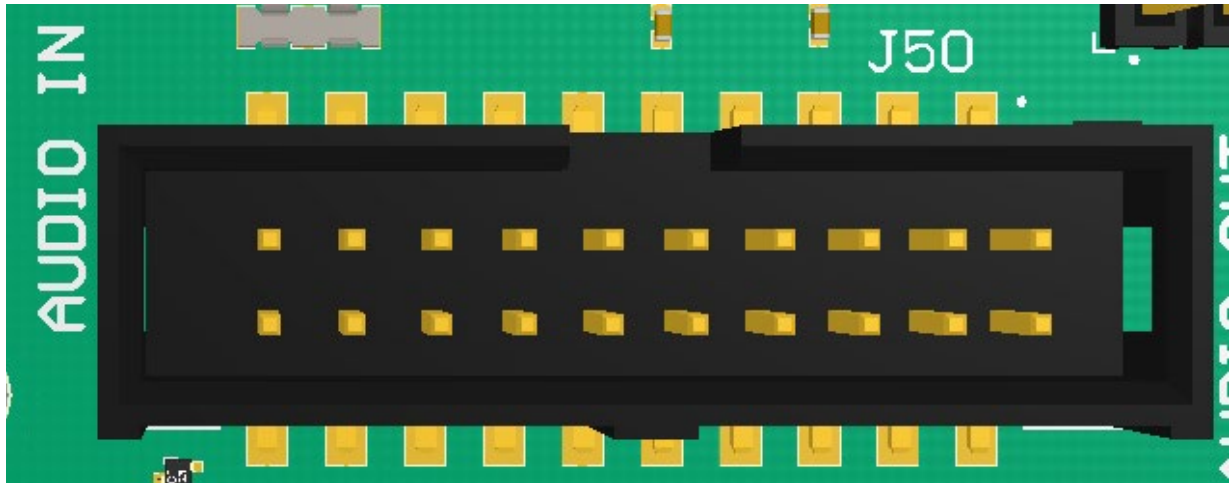


Figure 14 ANC Headphone Jack

The ANC headset jack (J27) is a special 3.5mm TRRS jack with ANC capabilities. It is backwards compatible with standard headset jacks. Please contact Lantronix at [sales@lantronix.com](mailto:sales@lantronix.com) for compatible ANC headsets.



### 3.8.12 Audio Inputs Expansion Header J50



**Figure 15 J50 Audio Inputs Expansion Header**

This header expansion provides the following audio inputs:

1. 3 digital mics
2. 3 analog mics
3. Voltage rails to support analog and digital mics

For details on how to connect analog or digital microphones to system, refer to sections 4.13.1 and 4.13.2 on Open-Q™\_820DevKit\_SOM\_TechNote13 (document R-3).

The table below outlines the pin out information of the audio inputs expansion header J50:

**Table 3.8-9 Audio Inputs Expansion Header J50 Pin out**

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog MIC1 positive differential input	CDC_IN1_P	J50[1]	Analog MIC1 negative differential input	CDC_IN1_N	J50[2]
Analog MIC5 positive differential input	CDC_IN5_P	J50[3]	Analog MIC5 negative differential input	CDC_IN5_N	J50[4]
MIC bias output voltage 1	MIC_BIAS1	J50[5]	MIC bias output voltage 3	MIC_BIAS3	J50[6]
Analog MIC6 positive differential input	CDC_IN6_P	J50[7]	Analog MIC6 negative differential input	CDC_IN6_N	J50[8]
MIC bias output voltage 4	MIC_BIAS4	J50[9]	3.3V power supply max 500mA	MB_VREG_3P3	J50[10]
GND	GND	J50[11]	GND	GND	J50[12]

Description	Signal	Pin NO	Description	Signal	Pin NO
Clock for digital MIC 1 and 2	CDC_DMIC_CLK0	J50[13]	Clock for digital MIC 3 and 4	CDC_DMIC_CLK1	J50[14]
Digital MIC 1 and 2 data line	CDC_DMIC_DATA0	J50[15]	Digital MIC 3 and 4 data line	CDC_DMIC_DATA1	J50[16]
1.8V power supply max 300mA	VREG_S4A_1P8	J50[17]	Clock for digital MIC 5 and 6	CDC_DMIC_CLK2	J50[18]
GND	GND	J50[19]	Digital MIC 5 and 6 data line	CDC_DMIC_DATA2	J50[20]

### 3.8.13 Audio Outputs Expansion Header J26

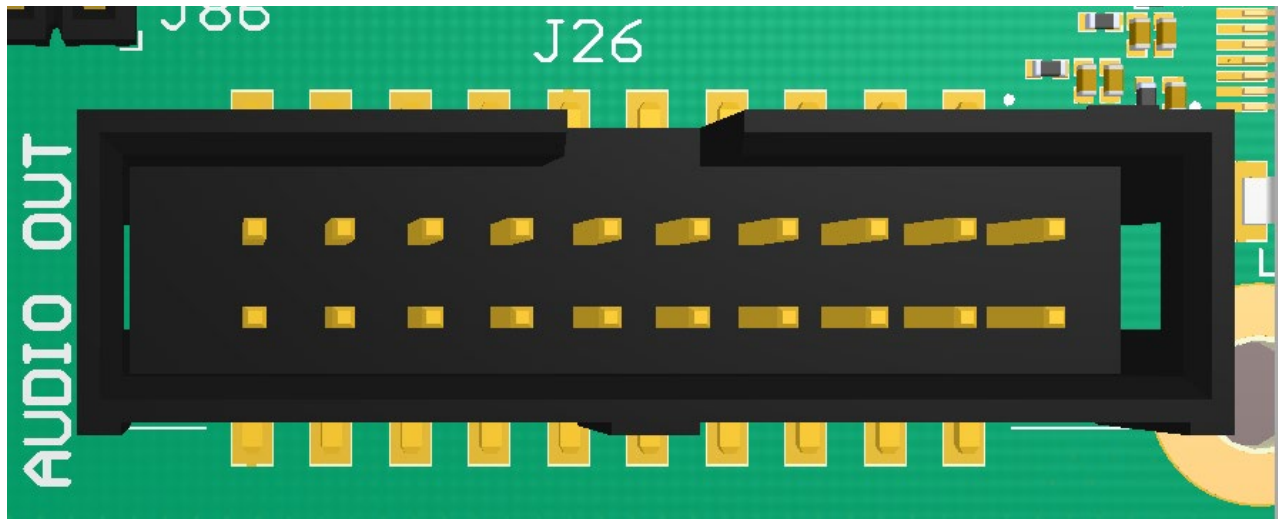


Figure 16 J26 Audio Outputs Expansion Header

This header expansion provides the following audio outputs:

1. 2 differential analog audio line out
2. 2 single ended analog audio line out
3. 1 differential analog earpiece amplifier output (no external amp needed)
4. 2 speaker amplifier enable control
5. Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio outputs expansion header J26:

**Table 3.8-10 Audio Outputs Expansion Header J26 Pin out**

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog audio line out 1, positive differential output	CDC_LINE_OUT1_P	J26[1]	Analog audio line out 1, negative differential output	CDC_LINE_OUT1_N	J26[2]
Analog audio line out 2, positive differential output	CDC_LINE_OUT2_P	J26[3]	Analog audio line out 2, negative differential output	CDC_LINE_OUT2_N	J26[4]
Audio line outputs 3 and 4 GND reference	CDC_LINE_REF	J26[5]	3.3V output power supply	MB_VREG_3P3	J26[6]
Analog audio line out 3, single ended output	CDC_LINE_OUT3	J26[7]	Analog audio line out 4, single ended output	CDC_LINE_OUT4	J26[8]
Analog earpiece amplifier out, positive differential output	CDC_EAR_P	J26[9]	Analog earpiece amplifier out, negative differential output	CDC_EAR_N	J26[10]
GND	GND	J26[11]	3.8V output power supply	MB_VREG_SOM	J26[12]
Digital sound wire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_CLK	J26[13]	Digital sound wire data for WSA8810/ WSA8815 smart speaker amplifier	CDC_SWR_DATA	J26[14]
Speaker amplifier enable 1	SPKR_AMP_EN1	J26[15]	Speaker amplifier enable 2	SPKR_AMP_EN2	J26[16]
1.8V output power supply	VREG_S4A_1P8	J26[17]	12V output power supply	DC_IN_12V	J26[18]
5.0V output power supply	MB_VREG_5P0	J26[19]	GND	GND	J26[20]

### 3.8.14 On Board PCB WLAN Antennas

The Open-Q™ 820 carrier board has two on board WLAN PCB antennas that connects to the QCA6174 WiFi module on the SOM via coaxial cables that attaches to MHF4L receptacles. These antennas connect to the SOM in the following configuration:

- WLAN1 on the carrier board connects to ANT1 on the QCA6174 WiFi module
- WLAN0 on the carrier board connects to ANT2 on the QCA6174 WiFi module

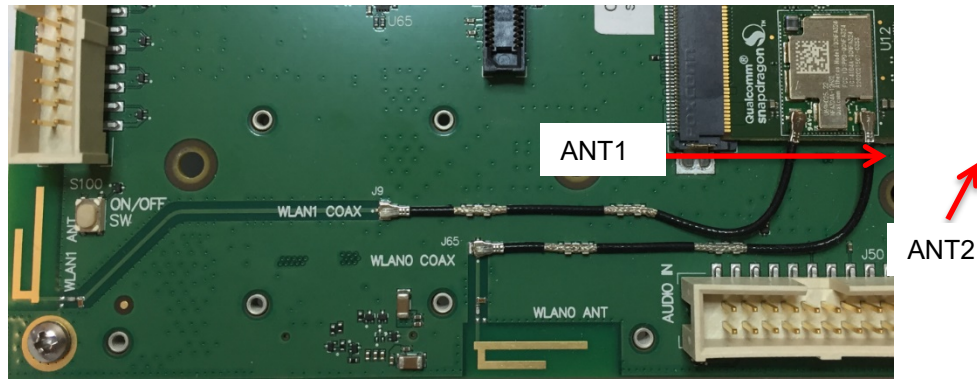


Figure 17 On Board PCB Antennas

### 3.8.15 External and on Board PCB GPS Antenna

The Open-Q™ 820 carrier board allows user the flexibility of using an external (via SMA connector) or an on board PCB GPS antenna. Depending on which antenna is used, dip switch S10 needs to be configured (see table below for details).

GPS Antenna Selection	Dip Switch S10 (Position 8) Selection
On Board PCB Antenna	Off Position
External Antenna (Passive Antenna Only)	On Position

If an external GPS antenna is preferred, Lantronix recommends the Laird Technologies hepta-band dipole antenna (manufacture part number: MAF94300). It is important to note that GPS should be used or tested near a window or a location where satellites are easily “seen” by the device.

### 3.8.16 Open-Q Display

The display output options for the Open-Q 820 Development Kit consists of:

- An HDMI type A connector
- A 100-pin display connector J2 that supports:
  - Dual DSI DPHY 1.2 (up to 3840 x 2400 at 60 fps)
  - HDMI 2.0 (4K60) or 4K30 Miracast
  - Touch screen capacitive panels via I2C, SPI, and interrupts (up to two devices)
  - Backlight LED
    - Can support external backlight driver control and power
    - PMI8996 backlight driver supports four LED strings of up to 30mA each with 28V maximum boost voltage

The Open-Q development platform can support the following display combinations:

MIPI DSI	1 x 4lane DSI0 + 1 x 4lane DSI1 1 x 8 lane combining DSI0 and DSI1 for up to 4K resolution 2 x 4-lane DSI DPHY 1.2 and HDMI (4K60) or 4K30 Miracast
----------	---

	Display 3840 x 2400 at 60fps, 2560 buffer width (10 layers blending)
HDMI	V2.0 (4K60)

### 3.8.17 HDMI Connector J25

The on board HDMI type A connector enables the Open-Q development platform to connect to an external HDMI monitor/ television via an HDMI cable. As part of a new feature, the APQ8096 can now support up to 4K UHD (3840 x 2400 at 60fps) and HDMI 2.0 (4K60)/ 4K30 Miracast.

Please note that the Open-Q 820 Development kit is for evaluation purposes only and may not be HDMI compliant.

### 3.8.18 Display Connector J2

The 100-pin display connector provides the following features/ pin-outs that enables the development kit to connect to a MIPI DSI panel/ device:

**Note:** Please refer to the carrier schematic and display board tech notes when designing a custom display board.

- DSI
  - 2 x 4 lane DSI
- Backlight
  - Built-in backlight WLED driver on PMI8996
    - WLED driver supports up to 28.5V output for backlight
  - Primary external backlight (BL0)
    - Backlight control signals
    - External Power
  - Secondary external backlight (BL1)
    - Backlight control signals
    - External power
- Display connector – LCD/ AMOLED
  - PMI8996 programmable display bias output voltage:
    - 5V to 6.1V and -1.4V to -6.0V (LCD display)
    - 4.6V to 5V and -1.4V to -5.4V (AMOLED display)
- Additional GPIOs for general purposes available
- VREG\_S4A voltage rail from PM8996
  - Required by display for DOVDD
  - 300mA current path
- Touch Panel
  - Supports up to two touch screen controllers

- Supports I2C or SPI via BLSP1 and SSC\_5
- Can chose between I2C or SPI signals via MUX

#### Power specifications

The display connector supports the following power domains:

Display Signal	Power Domain
PM8996 LDO22 (3.3-2.8V)	up to 150 mA
PM8996 LDO14 (1.8V- 2.15V)	up to 150 mA
PM8996 LDO15(1.8V – 2.15V)	up to 300 mA
PM8996 S4A (1.8V)	up to 300 mA
Carrier 3.3V	up to 0.5A
Carrier 5 V	up to 1.5A
Carrier 12 V	up to 0.5A

The IOpen-Q 820 display board (part number: 225-0100) is an additional PCB that mates with the display connector J2 on the carrier board. This board allows users to interface with the development kit via the LCD (Truly display panel, see below for details) that comes preinstalled on the display board. Figure 18 illustrates the interfacing connectors on the display board. Note that there are two ERM8 connectors; J1 is for interfacing with the development kit via the LCD panel, while J7 allows users to access the display signals on the carrier board (display connector J2) via connector J8 on the display board.

**Note:** The display board comes as an additional add-on to the Open-Q 820 development kit. To purchase this, please visit <http://shop.intrinsyc.com> or contact Lantronix at [sales@lantronix.com](mailto:sales@lantronix.com) for details.

**Note:** Please refer to “Open-Q 820 (APQ8096) Development Kit Technical Note 15: Display Board Design Guide” for more information on designing a custom display board.

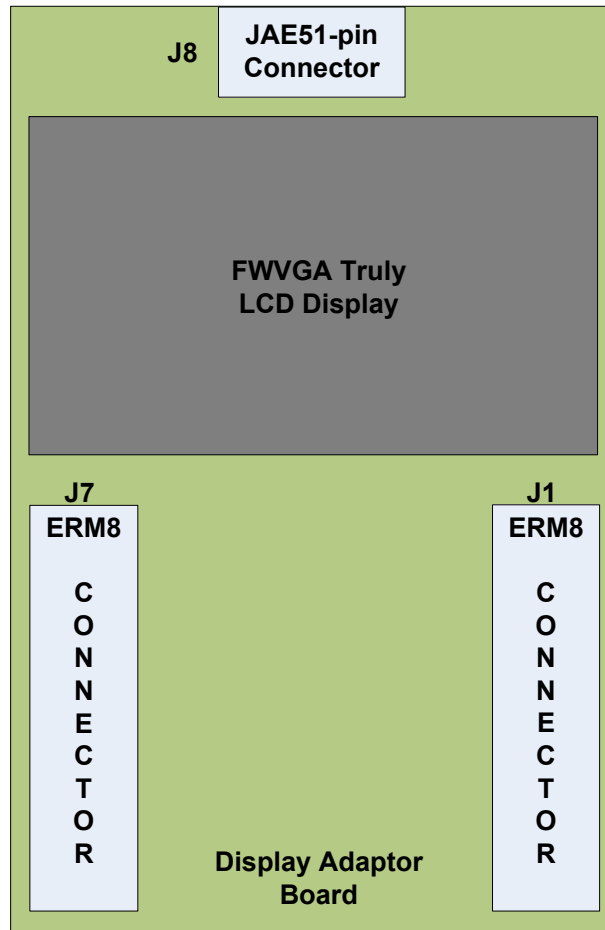


Figure 18 Display Board Block Diagram

### 3.8.18.1 Connecting the Display Board to the Development Kit

This configuration allows the user to use the preinstalled LCD display that comes with the display adaptor board. As shown in the block diagram below, the MIPI DSI0 lines, which come from the 100-pin ERM8 connector, directly connects to the FWVGA LCD panel. See the section below for more details on this LCD panel. It is important to note that connector J1 of the display board needs to connect to J2 of the carrier board for this configuration to work.

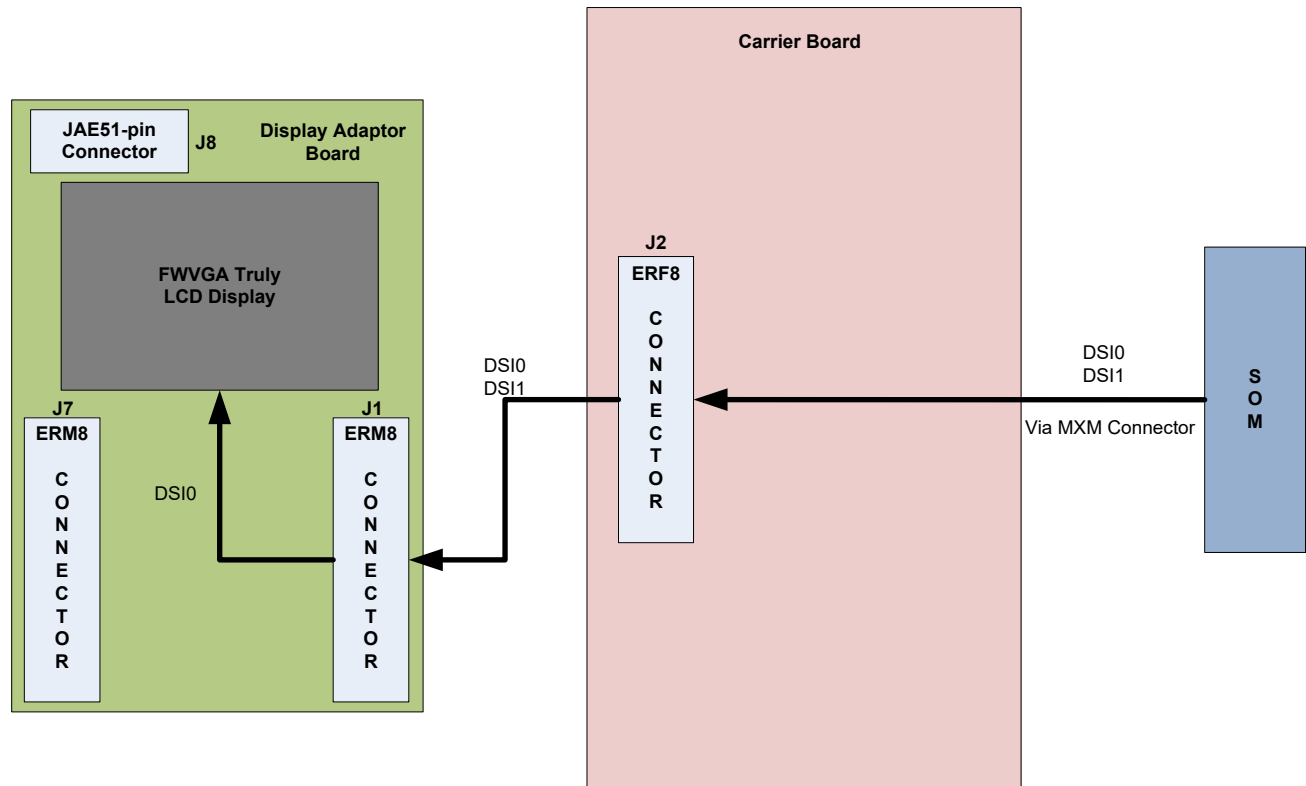


Figure 19 Display Board Default Configuration

### 3.8.18.2 Display Panel

This LCD panel comes preinstalled on the Open-Q 820 display adaptor board (part number: 225-0100). Below are the Panel specifications:

- Resolution: 480x854
- LCD Type: IPS
- PCAP touch panel with cover glass
- No of Lanes: 1 x 2 lane MIPI DSI interface via Display Board.
- Diagonal Length: 4.5"
- Contact [sales@lantronix.com](mailto:sales@lantronix.com) for more information

**Note:** The display above when mounted on the Open-Q 820 Display Adaptor is meant to work with the carrier board. Altering the use of this LCD panel is not recommended.

**Note:** 225-0100 display adaptor boards are currently end of life. The Open-Q 820 Display adapter board (part number: 280-0100) has the same specifications (as described above) and pin-outs as 225-0100.



### 3.8.19 PCI Express 1X Slot J30

The PCI Express slot (J30) used on the Open-Q 820 development kit is a standard PC style half-height card slot. It allows for external peripheral connectivity such as Gigabit Ethernet, Gigabit Wi-Fi, or PCIe based audio / video processors. Since there is no native Ethernet connectivity on the Open-Q platform, an off-the shelf PCIe based Ethernet card can be used here. Please check the software compatibility before connecting the PCIe Ethernet card. In addition to being able to establish external connectivity, the connector provides access to the PCIE2 interface, which is routed from the SOM.

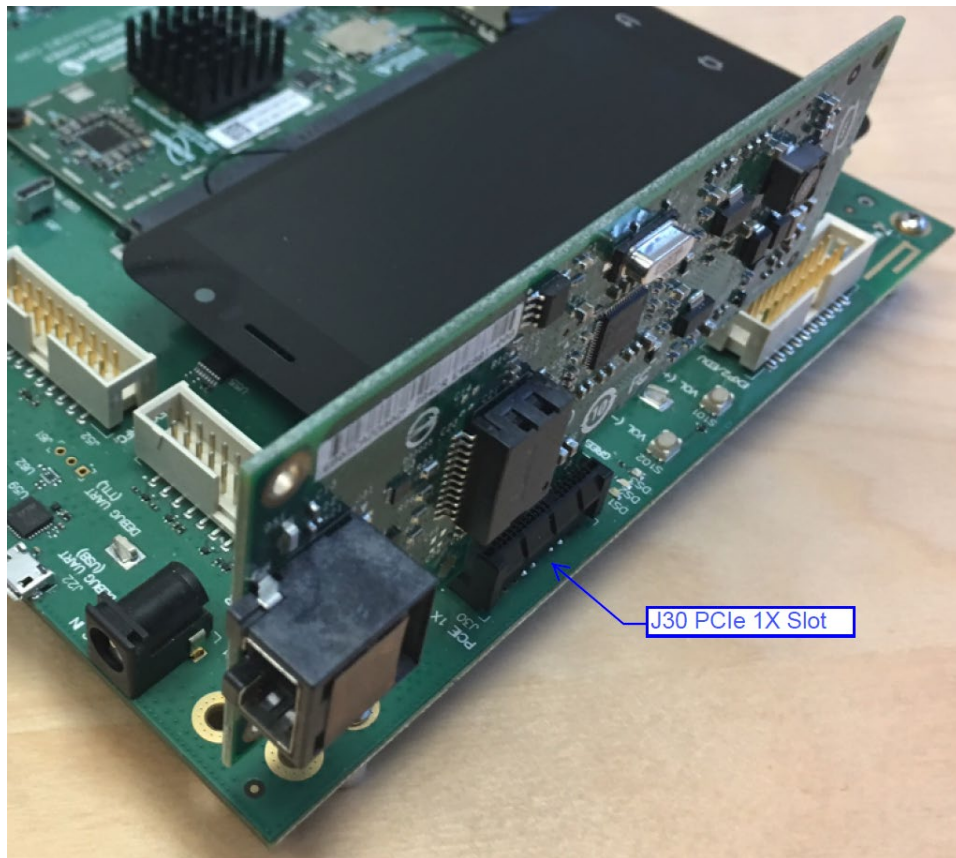


Figure 20 J30 PCIe Connector

### 3.8.20 Mini PCI Express Connector J72

The Open-Q 820 development kit also supports the use of a PCI Express mini card. The primary difference between a PCI Express 1X card and a PCI Express mini card is the unique form factor optimized for mobile computing platforms. In addition to that, the mini card is optimized for communication applications. Similarly, the PCI Express mini card allows for external peripheral connectivity such as Ethernet and wireless connectivity as well as acting like a modem.

The Mini PCI Express connector J72 used on the Open-Q 820 development kit supports both the standard full and half size PCI Express mini card. Depending on the size of card used, user can utilize the 4 mounting holes below connector J72 to secure the card in place. Figure 22 depicts these mounting holes. Please check the software compatibility before connecting any PCI Express mini cards.

**Note:** The pin-outs of this connector comply with the PCI Express mini card standards. Please refer to the document at the following link for more information:

<https://www.pcisig.com/specifications/pciexpress/base/#mini1.2>

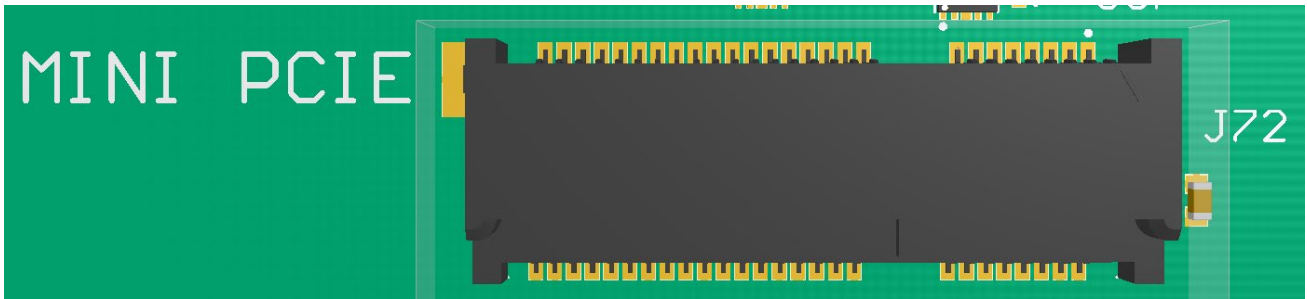


Figure 21 J72 Mini PCIe Connector

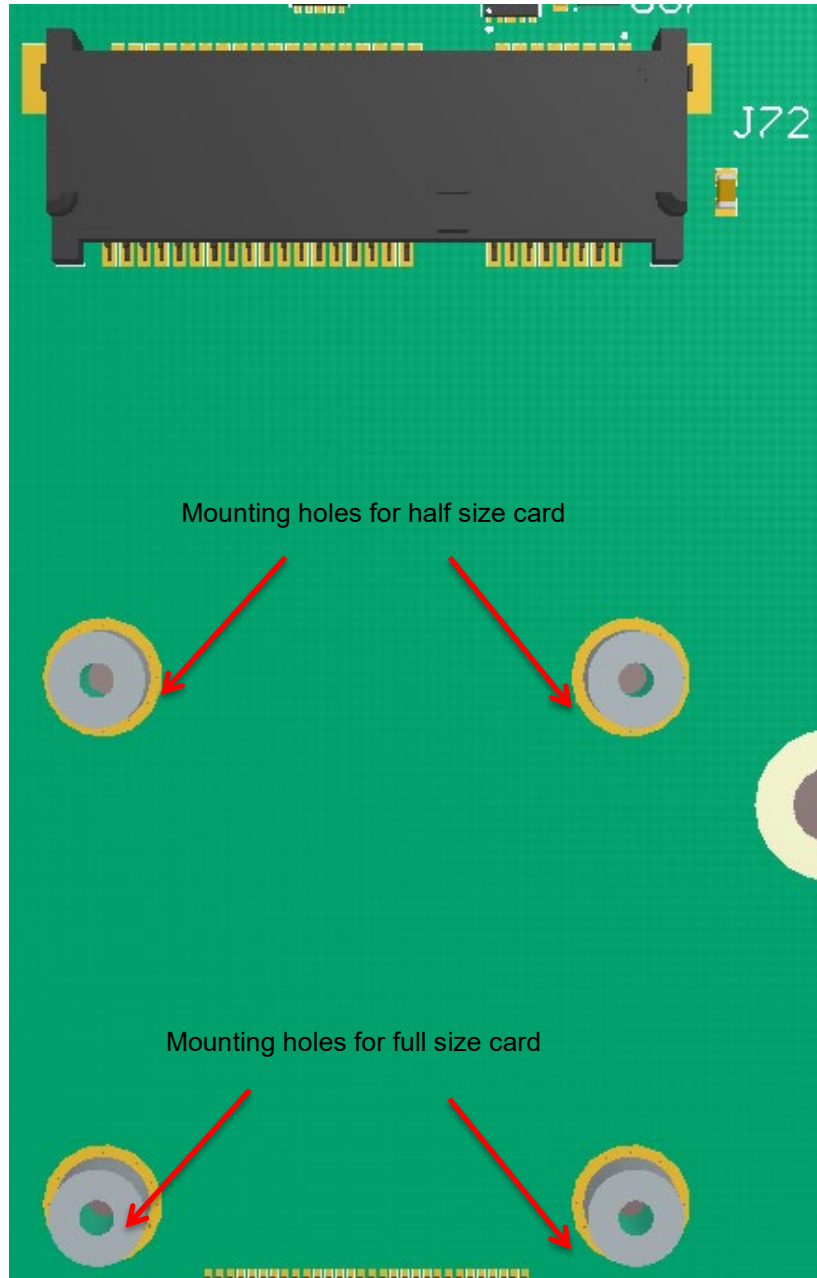


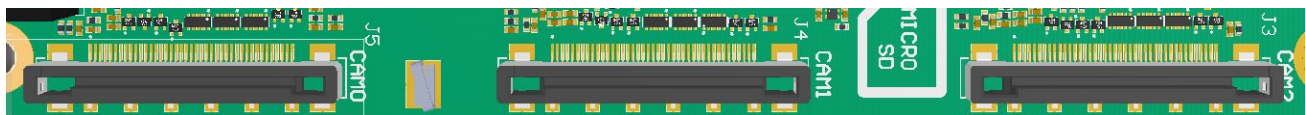
Figure 22 J72 Mounting Holes for Mini PCIe Connector

### 3.8.21 Camera Connectors

The Open-Q 820 development kit supports three 4-lane MIPI camera interfaces via three separate JAE 41-pin connectors.

The following are some features of the camera connectors:

- 3 x 4 lane MIPI CSI signals
- No support for integrated flash driver
- Support for 3D camera configuration
  - Separate I2C control (CCI0, CCI1)
- Supports all CSI interfaces
- All camera CSI connectors are on the carrier board edge
- Self-regulated camera modules can be powered with 3.3V power (MB\_VREG\_3P3)
- Uses JAE FI-RE41S-VF connector for exposing MIPI, CLK, GPIOs and Power rails.
- Please use JAE FI-RE41S-VF connector to access signals such as MIPI, CLK, GPIO and power rails



**Figure 23 Camera Connectors (J5,J4,J3)**

Figure 23 above shows the three MIPI CAM0 (J5), CAM1 (J4) and CAM2 (J3) connectors. Table 3.8.21-1 below outlines the pin outs of these connectors

**Table 3.8.21-1. MIPI CSI Camera Connector Pin outs (J5,J4,J3)**

Pin#	CAM0(J5)	CAM1(J4)	CAM2(J3)	Description
1,2,3	MB_VREG_3P3	MB_VREG_3P3	MB_VREG_3P3	Power output. Connected to main +3.3V MB_VREG_3P3 max current 700mA
4	GND	GND	GND	Ground
5	VREG_L17A_2P8	VREG_L18A_2P8	VREG_L29A_2P8	Power output. Connected to various PM8996 LDO regulators. Default is +2.8V. Maximum current 300mA
6	MB_ELDO_CAM0_DVDD	MB_ELDO_CAM1_DVDD	MB_ELDO_CAM2_DVDD	Power output. Connected to U5, U6, and U71 AMS LDO regulator. Default is +1.2V. Maximum current 500mA
7,8	VREG_L23A_2P8	MB_ELDO_CAM1_VCM	VREG_L23A_2P8	Power output. Connected to PM8996 VREG_L23A regulator or on board LDO regulator. Default is +2.8V. Maximum current 300mA

Pin#	CAM0(J5)	CAM1(J4)	CAM2(J3)	Description
9,10	VREG_LVS1A_1P8	VREG_LVS1A_1P8	VREG_LVS1A_1P8	Power output. Connected to PM8996 VREG_LVS1A switch output. Default is +1.8V. Maximum current 300mA
11	GND	GND	GND	Ground
12	FLASH_STROBE_EN (APQ_GPIO21)	FLASH_STROBE_EN (APQ_GPIO21)	FLASH_STROBE_EN (APQ_GPIO21)	Output. Connected to APQ8096. Default use is for camera flash strobe enable
13	CAM0_RST_N (APQ_GPIO25)	CAM1_RST_N (APQ_GPIO104)	CAM2_RST_N (APQ_GPIO23)	Output. Connected to APQ8096. Default use is for camera reset
14	CAM0_STANDBY_N (APQ_GPIO26)	CAM1_STANDBY_N (APQ_GPIO98)	CAM2_STANDBY_N (APQ_GPIO133)	Output. Connected to APQ8096. Default use is for camera standby
15	CCI_I2C_SCL0 (APQ_GPIO18)	CCI_I2C_SCL0 (APQ_GPIO18)	CCI_I2C_SCL0 (APQ_GPIO18)	Output. Connected to APQ8096. Default use is for camera CCI0 I2C clock interface (this is not a generic I2C port).
16	CCI_I2C_SDA0 (APQ_GPIO17)	CCI_I2C_SDA0 (APQ_GPIO17)	CCI_I2C_SDA0 (APQ_GPIO17)	Input / output. Connected to APQ8096. Default use is for camera CCI0 I2C data interface (this is not a generic I2C port).
17	CAM_MCLK0_BUF (APQ_GPIO13)	CAM_MCLK1_BUF (APQ_GPIO14)	CAM_MCLK2_BUF (APQ_GPIO15)	Output. Connected to APQ8096. Default use is for camera master clock. Maximum 24MHz
18	FLASH_STROBE_TRIG (APQ_GPIO22)	FLASH_STROBE_TRIG (APQ_GPIO22)  Install R37 to access signal	FLASH_STROBE_TRIG (APQ_GPIO22)  Install R43 to access signal	Output. Connected to APQ8096. Default use is for camera flash strobe trigger
19	GND	GND	GND	Ground
20	MIPI_CSI0_LANE0_N	MIPI_CSI1_LANE0_N	MIPI_CSI2_LANE0_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
21	MIPI_CSI0_LANE0_P	MIPI_CSI1_LANE0_P	MIPI_CSI2_LANE0_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
22	GND	GND	GND	Ground
23	MIPI_CSI0_CLK_N	MIPI_CSI1_CLK_N	MIPI_CSI2_CLK_N	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
24	MIPI_CSI0_CLK_P	MIPI_CSI1_CLK_P	MIPI_CSI2_CLK_P	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
25	GND	GND	GND	Ground

Pin#	CAM0(J5)	CAM1(J4)	CAM2(J3)	Description
26	MIPI_CSI0_LANE1_N	MIPI_CSI1_LANE1_N	MIPI_CSI2_LANE1_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
27	MIPI_CSI0_LANE1_P	MIPI_CSI1_LANE1_P	MIPI_CSI2_LANE1_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
28	GND	GND	GND	Ground
29	MIPI_CSI0_LANE2_N	MIPI_CSI1_LANE2_N	MIPI_CSI2_LANE2_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
30	MIPI_CSI0_LANE2_P	MIPI_CSI1_LANE2_P	MIPI_CSI2_LANE2_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
31	GND	GND	GND	Ground
32	MIPI_CSI0_LANE3_P	MIPI_CSI1_LANE3_P	MIPI_CSI2_LANE3_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
33	MIPI_CSI0_LANE3_N	MIPI_CSI1_LANE3_N	MIPI_CSI2_LANE3_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
34	GND	GND	GND	Ground
35	CCI_I2C_SDA1 (APQ_GPIO19)	CCI_I2C_SDA1 (APQ_GPIO19)	CCI_I2C_SDA1 (APQ_GPIO19)	Output / Input. Connected to APQ8096 GPIO19. Default use is for camera CCI1 I2C data interface
36	CCI_I2C_SCL1 (APQ_GPIO20)	CCI_I2C_SCL1 (APQ_GPIO20)	CCI_I2C_SCL1 (APQ_GPIO20)	Output. Connected to APQ8096 GPIO20. Default use is for camera CCI1 I2C clock interface
37	CAM_IRQ (APQ_GPIO24)	CAM_IRQ (APQ_GPIO24)  Install R40 to access signal	CAM_IRQ (APQ_GPIO24)  Install R46 to access signal	Input. Connected to APQ8096 GPIO24. CAM_IRQ signal
38	CAM0_MCLK3 (APQ_GPIO16)  Install R16 to access signal	CAM1_MCLK3 (APQ_GPIO16)	CAM2_MCLK3 (APQ_GPIO16)  Install R47 to access signal	Output. Connected to APQ8096 GPIO16. Default use is for camera master clock. Maximum 24MHz
39	GND	GND	GND	Ground
40,41	MB_VREG_5P0  Install R10 to access signal	MB_VREG_5P0  Install R28 to access signal	MB_VREG_5P0  Install R35 to access signal	Power output. 5V Power supply. Maximum 700mA

**Note:** A connection from the camera connectors on the carrier board to the camera adapter board is established by a 41-pin cable assembly from JAE Electronics (part number JF08R0R041020MA)

The table below shows the combinations of camera usage for different use cases

Table 3.8.21-2. MIPI CSI Camera Use Cases

CSI PHY	Use case	Comment
CSI0	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 1	Up to 4 lane	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 2	Up to 4 lane	One Camera of 4 lane or 2 x Camera of 1 lane each
CSI0 + CSI1	Up to 4 lane 3D	4 lane 3D use case / Dual 4 lane configuration
CSI 2	Up to 1 lane 3D	1 lane 3D use case / Dual 1 lane configuration
CSI0 + CSI1 + CSI2	Up to 4 lane	Three 4-lane CSI (4+4+4 or 4+4+2+1)
CPHY		Three 3-trio CPHY1.0

### 3.8.22 Power Header via 20 Pin Connector J60

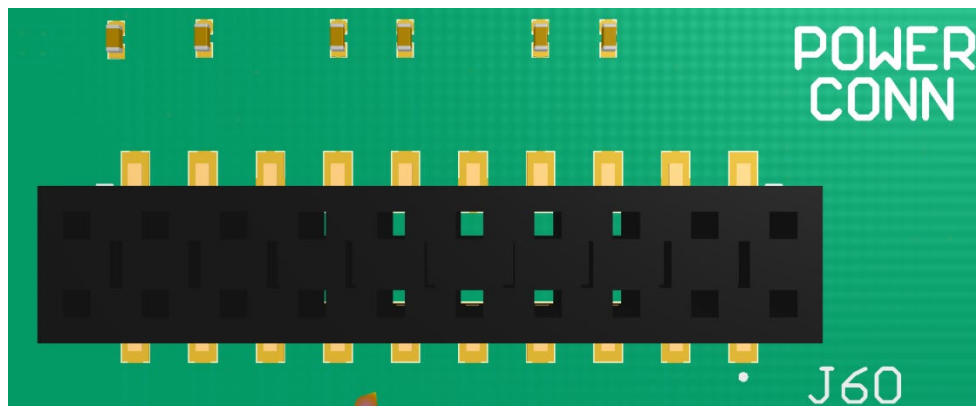


Figure 24 J60 Power Connector

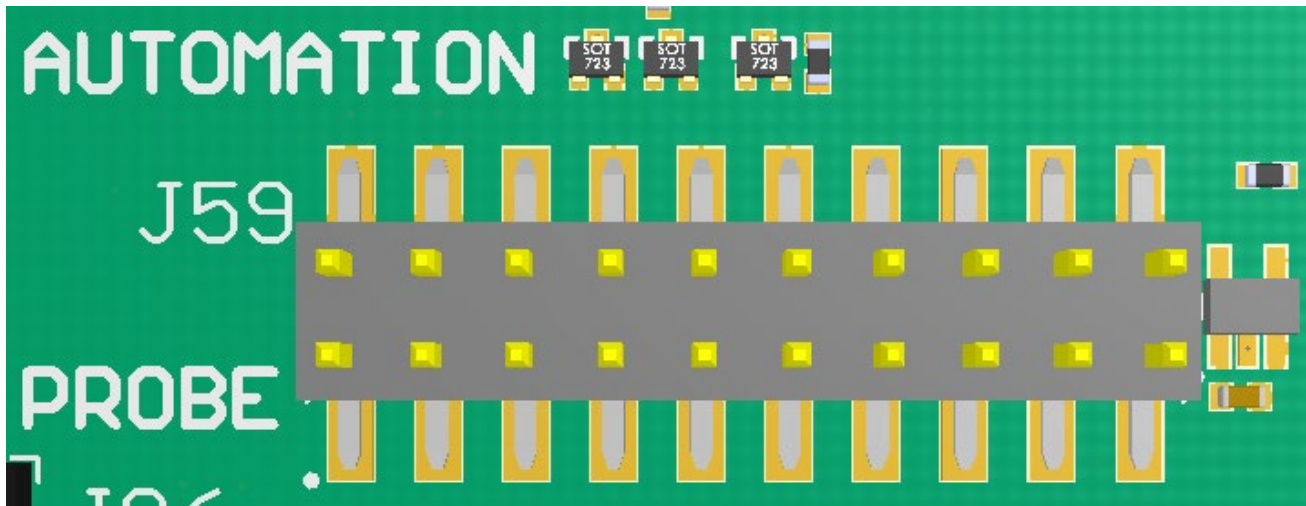
- For providing camera connectors with additional current than what is originally supported by on board regulators. This is to mitigate the effect of high resistance and IR drop on flat cables which can violate camera sensor requirements for high performance cameras
- It is recommended to use this when high performance (high mega pixels) cameras are being used. Usually high performance cameras require more power
- Can be used as a general power header if user would like to use voltage rails brought out by connector

Table 3.8.22-1. Power Header J60 Pin-out

Description	Signal	Pin NO	Description	Signal	Pin NO
1.05V power rail for camera 0	MB_ELDO_CAM0_DVDD	J60[1]	2.85V power rail for camera 0 (AVDD)	VREG_L17A_2P8	J60[2]
2.8V power rail for camera 0, 2 (VDD)	VREG_L23A_2P8	J60[3]	GND	GND	J60[4]
GND	GND	J60[5]	3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[6]
1.05V power rail for camera 1	MB_ELDO_CAM1_DVDD	J60[7]	2.85V power rail for camera 1 (AVDD)	VREG_L18A_2P85	J60[8]
2.8V power rail for camera 1 (VDD)	MB_ELDO_CAM1_VCM	J60[9]	GND	GND	J60[10]
GND	GND	J60[11]	3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[12]
1.05V power rail for camera 2	MB_ELDO_CAM2_DVDD	J53[13]	2.85V power rail for camera 2 (AVDD)	VREG_L29A_2P8	J60[14]
2.8V power rail for camera 0, 2 (VDD)	VREG_L23A_2P8	J53[15]	GND	GND	J60[16]
1.8V power rail for camera 0, 1, 2	VREG_LVS1A_1P8	J60[17]	3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[18]
5V power rail for camera 0, 1, 2	MB_VREG_5P0	J60[19]	12V power rail for camera 0, 1, 2	DC_IN_12V	J60[20]



### 3.8.23 Automation Connector Header J59



**Figure 25 J59 Automation Connector Header**

This header is used for automating tests on the development platform. Such tests include powering on and off and managing automated software downloads on the board. If automation is not required, user can access free GPIO pins from this header. Table 3.8.23-1 below outlines the pins that are available via header J59. Please refer to carrier and SOM schematics for details on where signals are connected to.

**Table 3.8.23-1. General System J59 Pin Out**

Description	Signal	Pin NO	Description	Signal	Pin NO
Power rail to support I2C signals coming from an external source	CONFIG_I2C_PWR	J26[1]	GND	GND	J26[2]
I2C clock signal from external source to Semtech GPIO expander	CONFIG_I2C_SCL	J26[3]	GND	GND	J26[4]
I2C data line to Semtech GPIO expander	CONFIG_I2C_SDA	J26[5]	Positive power sense line from Arm Energy Probe J86	SOM_PWR_SENSE_P	J26[6]
Negative power sense line from Arm Energy Probe J86	SOM_PWR_SENSE_N	J26[7]	When asserted high, this net drives the PON hardware signal input (BTN_PHONE_ON_N) low, initiating the PON sequence.	TC_START	J26[8]
When asserted high, this net drives the PMI8996 hardware input reset signal (BTN_RESET_N) low	TC_RESET	J26[9]	When asserted high, this net drives the system power off net (SYS_PWR_OFF_N) low.	TC_POWER_OFF	J26[10]

Description	Signal	Pin NO	Description	Signal	Pin NO
USB boot	FORCED_USB_BOOT	J26[11]	USB VBUS enable. Activating ESD protection circuit when asserted low	USB_VBUS_DIS_N	J26[12]
NC	NC	J26[13]	NC	NC	J26[14]
NC	NC	J26[15]	Chip reset input	APQ_RESOUT_N	J26[16]
NC	NC	J26[17]	NC	NC	J26[18]
NC	NC	J26[19]	GND	GND	J26[20]

### 3.8.24 Ethernet AVB Expansion Header J73

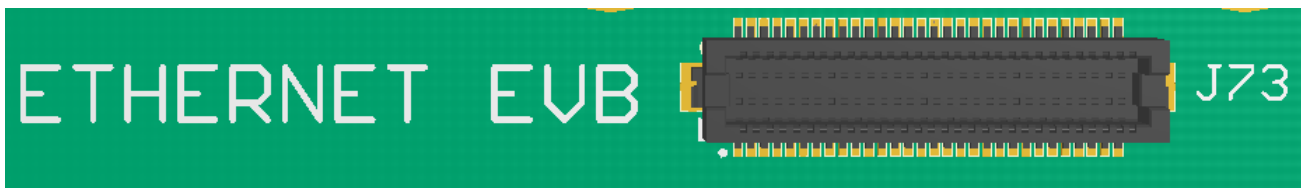


Figure 25 J73 Ethernet AVB Expansion Header

This header is used for interfacing with automotive peripherals via Ethernet AVB standard. Note that this is used for Lantronix internal testing and is not supported.

### 3.8.25 VIP Expansion Header J71

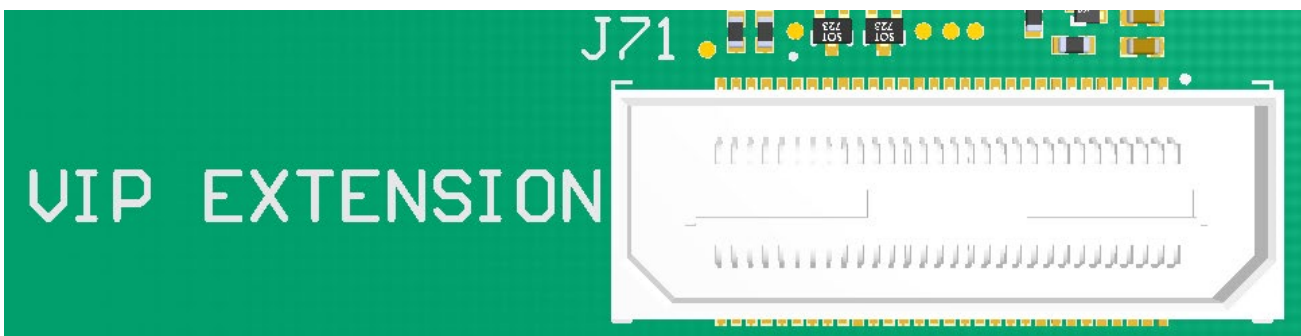


Figure 26 J71 VIP Expansion Header

This header is used for interfacing with Qualcomm legacy automotive VIP boards. Note that this is for Lantronix internal testing and is not supported.