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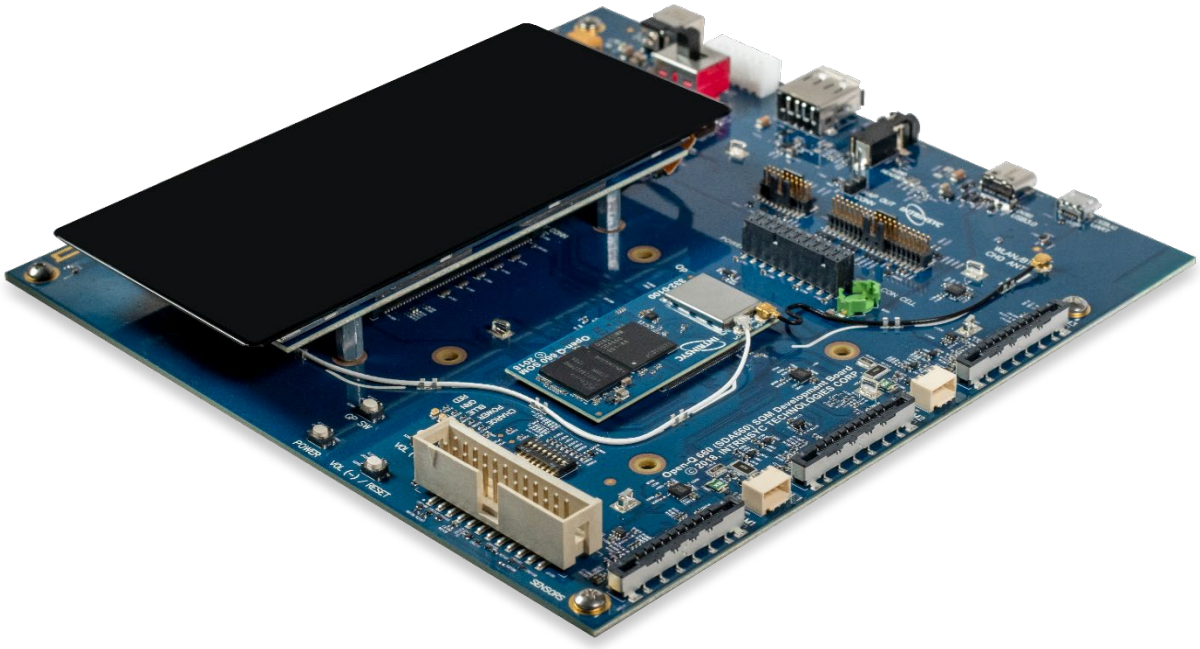

Open-Q™ 660 µSOM Development Kit User Guide

Part Number PMD-00083

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Revision History

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April 2019	1.0	Initial release. Intrinsyc document number: ITC-01RND1336-UG-001
October 2020	A	Initial Lantronix document. Added Lantronix document part number, Lantronix logo, branding, contact information, and links.

For the latest revision of this product document, please go to: http://tech.intrinsyc.com.

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1 Introduction

1.1 Purpose

The purpose of this user guide is to provide instructions and technical information on the Open-Q 660 µSOM Development Kit.

You can find information on this and other Lantronix development kits on the Lantronix web site: https://www.lantronix.com/products/open-q-660-usom-development-kit/

1.2 Scope

This document will cover the following items on the Open-Q 660 µSOM Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- SOM
- Carrier Board
- Available peripherals

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Lantronix Open-Q 660 µSOM Development Kit.

2 Documents

This section lists the supplementary documents for the Open-Q 660 µSOM Development Kit.

Applicable Documents

Reference	Title
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.1 Reference Documents

The below listed documents are available on the Lantronix Technical Portal: https://tech.intrinsyc.com (dev kit registration required).

Reference	Title
R-1	Open-Q 660 µSOM HW Device Specification
R-2	Open-Q 660 µSOM – Carrier Board Design Guide
R-3	Open-Q 660 µSOM Schematics (SOM and Carrier)
R-4	Open-Q 660 µSOM Development Kit – Display Adapter Design Guide
R-5	Open-Q 660 µSOM Development Kit – Camera Adapter Design Guide

2.2 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory

Term and acronyms	Definition
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SOM	System on Module
SPMI	System Power Management Interface (Qualcomm PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

3 Open-Q 660 µSOM Development Kit

3.1 Introduction

The Open-Q 660 provides a quick reference and evaluation platform for the Qualcomm Snapdragon SDA660 Platform. The development kit is suited for Android application developers, OEMs, consumer manufacturers, hardware component vendors, camera vendors, and product designers to evaluate, optimize, test and deploy applications that can utilize the Qualcomm Snapdragon SDA660 Platform technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at

http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 660 µSOM Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap.

3.4 Development Kit Contents

The Open-Q 660 µSOM Development Kit comes with Android software pre-programmed and includes the following:

  - Open-Q 660 µSOM with the Snapdragon 660 (SDA660) processor

- Mini-ITX form-factor carrier board
- AC power adapter

3.4.1 Important Locations

The diagram below shows the locations of key components, interfaces, and controls.

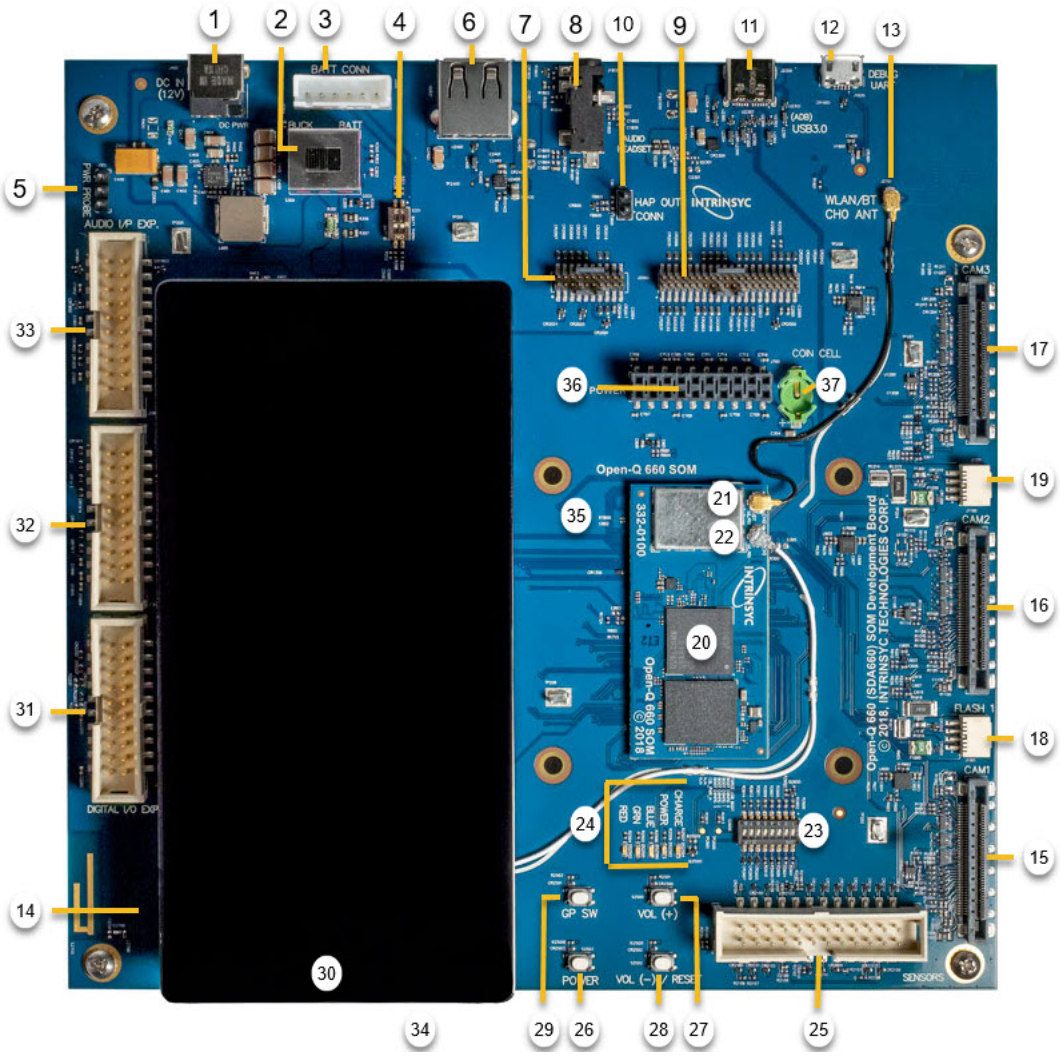


Figure 1. Assembled Open-Q 660 µSOM Development Kit

Table 1. List of Development Kit Features itemized in the figure above

Position	Feature Description	Reference Designator
1	DC Power Supply Jack	J400
2	Power Source Selector	S300
3	Battery Input Header	J300
4	Battery configuration DIP switch	S301
5	SOM Current Sense Probe Header	J301
6	USB 2.0 Type A Connector	J2400
7	Audio I/O Header #1	J2000
8	Audio Headset Jack	J1800
9	Audio I/O Header #2	J2001
10	Haptic Motor Header	J802
11	USB 3.0 Type-C connector for ADB	J2300
12	USB Serial Debug Console	J1600
13	WLAN/BT Channel 0 External Antenna Connector	J2701
14	WLAN Channel 1 External Antenna Connector	J2700
15	Camera 1 Connector	J1000
16	Camera 2 Connector	J1100
17	Camera 3 Connector	J1200
18	Flash 1 Header	J1001
19	Flash 2 Header	J1201
20	Open-Q 660 µSOM	
21	Open-Q 660 µSOM, WLAN/BT CH0 Antenna Connector	J2200
22	Open-Q 660 µSOM, WLAN CH1 Antenna Connector	J2201
23	System Configuration DIP Switch	S2600

24	LED Charge	DS2504
24	LED Power	DS2503
24	LED Blue	DS2500
24	LED Green	DS2501
24	LED Red	DS2502
25	Sensors Expansion Header	J2100
26	Button Power	S2503
27	Button Volume +	S2500
28	Button Volume -	S2502
29	Button GP SW	S2501
30	Open-Q LCD Panel	
31	Digital IO Expansion Header	J2200
32	Audio Outputs Expansion	J1901
33	Audio Inputs Expansion	J1900
34	Micro SD card socket	J1500
35	On-Board Quiet Thermistor	RT800
36	Power Header	J700
37	Coin Cell Holder	B300

3.4.2 Block Diagram

The block diagram below shows the connectivity and major components of the Open-Q 660 µSOM Development Kit.

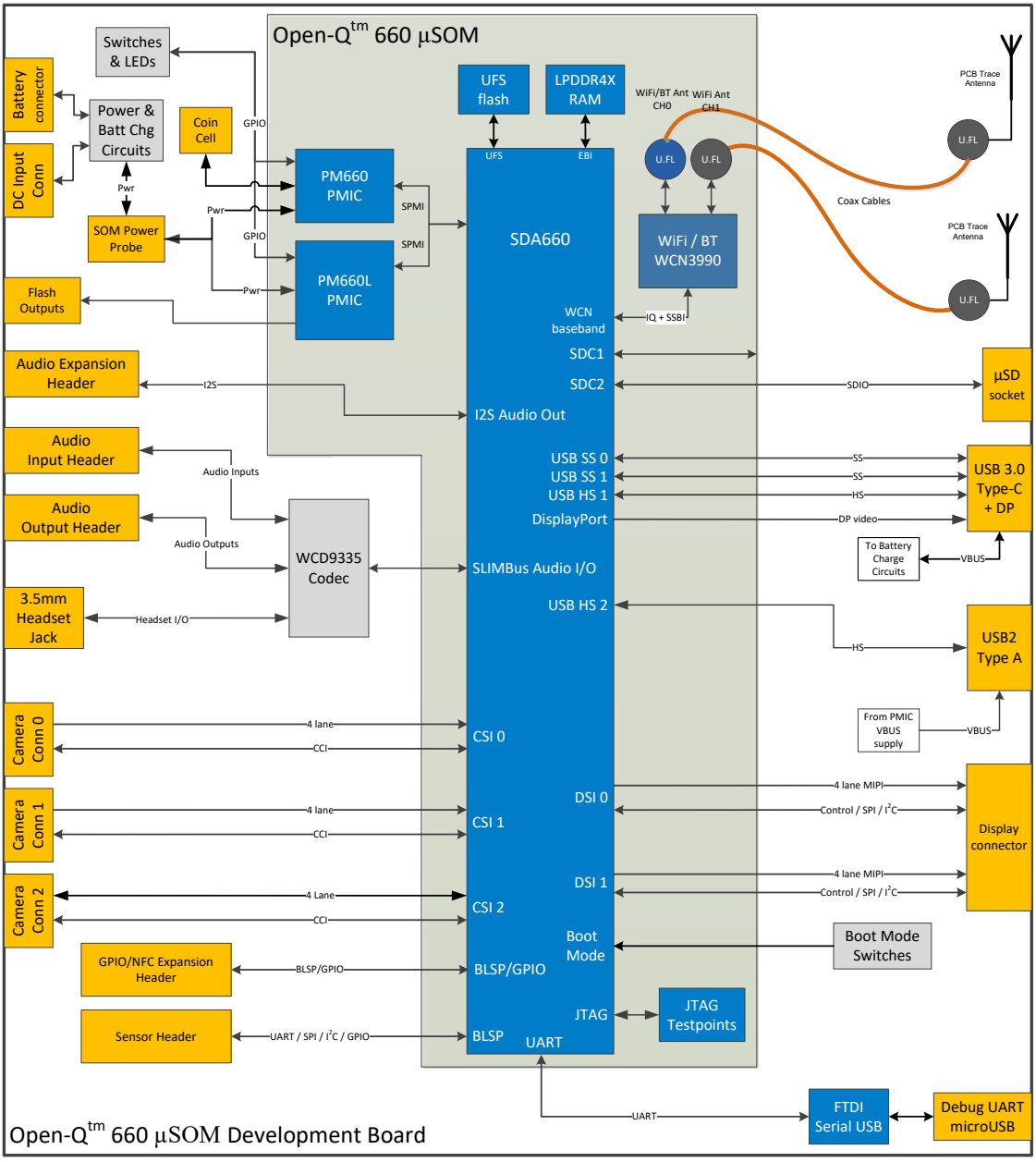


Figure 2. Open-Q 660 µSOM Dev Kit Block Diagram

3.4.3 Optional Accessories

Optional accessories are available for the Open-Q 660 µSOM Development Kit, like LCD Panel, Camera adapter, and sensor board. Please visit the Lantronix product store for availability of these accessories: http://shop.intrinsyc.com, or contact sales.

3.5 Getting Started

This section explains how to setup the Open-Q 660 µSOM Development Kit and start using it.

3.5.1 Registration

To register the development kit and gain access to the Lantronix Technical Document Portal, please visit: https://tech.intrinsyc.com/account/register.

To proceed with registration, the development kit serial number is required. These serial numbers can be found on the labels that are present on the SOM and carrier boards. The labels contain the following information:

- SOM: Serial Number, WIFI MAC address
- Carrier: Serial Number

Note: Please retain the SOM and carrier board serial numbers for warranty purposes.

Refer to http://tech.intrinsyc.com/projects/serialnumber/wiki for more details about locating the development kit serial number.

3.5.2 Configuration Switch Settings

The default configuration for the system configuration DIP switch S2600 is for all switches to be open or OFF. For details about other configurations, see section 3.7.2.

3.5.3 Powering Up the Development Kit

The development kit can be powered up by either using a DC power supply or by connecting a battery on the connector J400. Select the desired power source using the switch S300 on the carrier board. The green LED DS2503 marked “POWER” on the board is the power LED and should glow once the development kit is powered. To see the debug logs, connect a serial debug cable to the J1600 connector.

To power-up the board, perform the following exact steps below detailed below:

1. At a static-safe workstation, remove the development kit board carefully from the anti-static bag.
2. Connect the Power Adapter to the 12V DC Jack J400 and then press and hold the power button until you see the Lantronix logo appears on the on-board display (~3 seconds).
3. Navigate using the touchscreen on the on-board display.

3.6 Open-Q 660 µSOM

The Open-Q 660 µSOM contains the core Snapdragon 660 architecture. Measuring in at 50mm x 25mm, the SOM is where all the processing occurs. It is connected to the carrier board via three 100 pin Hirose DF40 connectors which allows essential power rails and signals to be exposed for supporting other peripherals and interfaces on the platform.

For detailed information about the Open-Q 660 µSOM, see the device specification noted as reference document R-1.

3.7 Open-Q 660 Carrier Board

The Open-Q 660 Carrier board is a Mini-ITX form factor board with various connectors used for connecting different peripherals. The table and sections below provide in depth information on the carrier board properties, user interfaces, connectors, and expansion headers found on the carrier board. This information is important for users wishing to connect other external hardware devices to the Open-Q 660 µSOM Development Kit. Users must ensure that before connecting any hardware device to the development kit, that it is compatible with the Open-Q 660 hardware specifications. See Figure 1 for position on carrier board.

Table 2. Carrier Board Features

Item	Position	Description	Specification	Usage
Form Factor		Dimensions: 170mm x 170mm	Mini-ITX Form Factor	
SOM Interface	20	3 x 100-pin Hirose DF40 connectors	SOM power and signal IO connection to carrier board.	The Open-Q 660 SOM connects to the carrier board through this interface.
Power	1	AC / Barrel charger	12 V DC Power Supply	Power Supply
Power	3	Battery connector for single cell lithium battery		Input power option
Debug Serial via USB	12	Debug Serial UART console over USB for development	USB Micro B connector	Development Serial Connector for debug output via USB
Buttons	29	General Purpose SW button	SMD Button	Additional button for general purpose
	26	Power Button	SMD Button	Power Button for Suspend / Resume and Power off
Volume Keys	27	Volume + key	SMD Button	Volume +Key
	28	Volume – key	SMD Button	Volume – Key
Sensor Connector	25	24 pin Sensor Expansion Connector		Available via Lantronix optional accessories kit
Digital IO Expansion Header	31	Exposes general purpose IO for user development		
Audio Headset Jack	8	Audio Headset Jack		Audio Headset
Audio Inputs Expansion	33	Audio Inputs Header	3 Analog Differential Inputs, 3 PDM Input Interfaces with phantom power	Microphones

Item	Position	Description	Specification	Usage
Audio Outputs Expansion	32	Audio Outputs Header	3 Line outputs, 1 earphone amplifier output	Amplifiers
Audio I/O	7, 9	2 x Audio I/O headers	3 x I2S, DMIC PDM, SPI/I2C interfaces	Various digital audio I/O functions
Haptic motor header	10	Haptic device driver	LRM and ERA capable output driver	Haptic motor
Micro SD (on bottom)	34	Micro SD card	4bit Micro SD card support	External Storage
USB Type C	11		USB type C connector	For USB debugging and client / host mode
USB Type A	6		Female Type A Connector	USB 2.0 Host interface
WLAN Antennas	13, 14	2 PCB Antennas		Coax connection to SOM WiFi module
Coin Cell Holder	37	Coin Cell battery holder provided	for PMIC RTC	
LEDs	24	Four LEDs	Two user driven LEDs	
LCD Display and Touch connector	30	100 pin for LCD signals	4-lane MIPI DSI MIPI Alliance Specification v1.01 MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01	For connecting display accessory
CSI Camera connectors	15, 16, 17	3 x camera connector	MIPI Alliance Specification v1.00 for Camera Serial Interface	For connecting camera accessories.
Flash driver	18, 19	2 x Flash drivers	Low current flash driver control	Flash control
Current Sense Header	5	3 pin header	Sense lines connected across 0.005 Ohm resistor	To measure current consumption of SOM

3.7.1 SOM Board to Board Connectors

The Open-Q 660 µSOM connects to the carrier board via three 100 pin Hirose DF40 connectors (20) which allows essential power rails and signals to be exposed for supporting other peripherals and interfaces on the platform. For the list of signals exposed by the SOM, see the device specification (Ref. R-1).

3.7.2 Configuration – DIP Switch S2600 (23)

There is a DIP switch S2600 on the top side of the Open-Q 660 carrier board. The 8-bit switch allows the user to control the system configuration and boot options. The image below shows the DIP switch assignments.

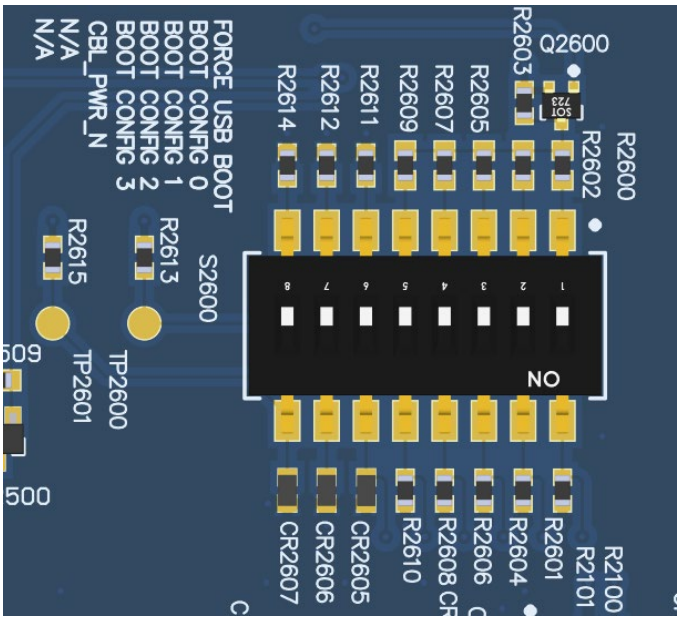


Figure 3. DIP switch assignments

See the table below for a description of the DIP switch connections.

Table 3 - System Configuration DIP Switch Settings

Function	DIP Switch	Description	Notes
FORCED_USB_BOOT	S2600-1	For factory mode programming. Connected to APQ GPIO57.	For Lantronix use only. Leave open / OFF.
WATCHDOG _DISABLE	S2600-2	Enables WATCHDOG_DISABLE when DIP switch turned on. Connected to APQ GPIO96	Unsupported feature. Leave switch open / OFF.
BOOT_CONFIG[1]	S2600-3	APQ boot configuration bit 1. Connected to APQ GPIO97	For default boot configuration, leave open / OFF. Other boot configurations not supported.
BOOT_CONFIG[2]	S2600-4	APQ boot configuration bit 2. Connected to APQ GPIO98	For default boot configuration, leave open / OFF. Other boot configurations not supported.

Function	DIP Switch	Description	Notes
BOOT_CONFIG[3]	S2600-5	APQ boot configuration bit 3. Connected to APQ GPIO60	For default boot configuration, leave open / OFF. Other boot configurations not supported.
CBL_PWN_N	S2600-6	Controls the auto power of the SOM.	Default configuration is open / OFF. To enable auto power on of the SOM, set switch closed / ON.
USR_DEBUG 1	S2600-7	User debug switch	Default out of the box configuration is OFF
USR_DEBUG 2	S2600-8	User debug switch	Default out of the box configuration is OFF

3.7.3 Input Power Selection (2)

The development kit can be powered using either external DC power supply or by using a battery. The input power source selection can be done using the power selection switch S300 as mentioned below.

3.7.3.1 Input Power Selection Switch S300 (2)

The S300 switch is used to select the power source. To select the external DC power supply as the power source, change the switch towards the BUCK position. To power up the kit using the battery, change the switch towards the BATT position. Default position is BUCK.

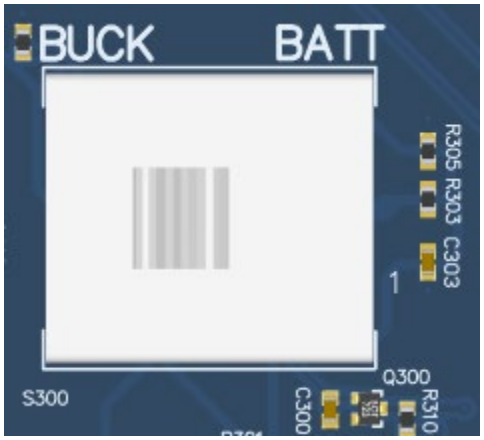


Figure 4. Power source selector switch S300 (2)

3.7.3.2 Battery ID and Thermistor Configuration DIP Switch S301 (4)

Battery ID and thermistor configuration is handled by the DIP switch S301. This switch has two sub switches, one is used for battery ID and another one is used for battery thermistor. The battery thermistor DIP switch should be closed to the ON position when power is supplied by the external power supply or when the connected battery does not have a built-in thermistor. The battery ID DIP switch should be closed to the ON

position when power is supplied by the external power supply or to force disabling of the SOM battery charger.

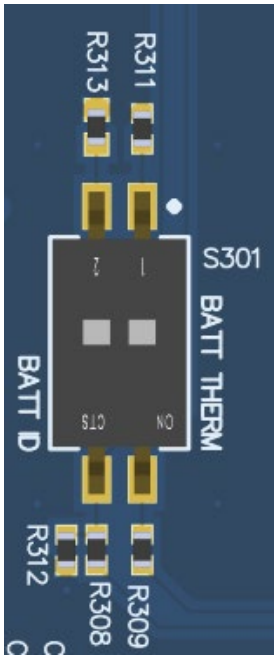


Figure 5. Battery ID and Thermistor DIP Switch S301 (4)

3.7.3.3 DC Power Input Jack J400 (1)

The Open-Q 660 µSOM Development Kit power source connects to the 12V DC power supply jack J400. Starting from the power jack, the 12V power supply branches off into different voltage rails via step down converters on the carrier board and PMIC on the SOM.

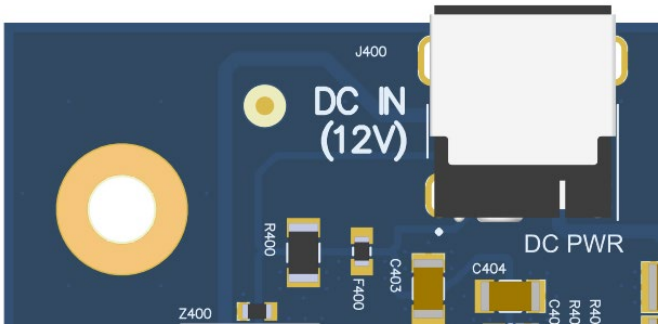


Figure 6. J400 12V DC Power Jack (1)

3.7.3.4 Battery Connector J300 (3)

The Open-Q 660 µSOM Development Kit can also be powered through a battery. Use the J300 connector on the carrier board to connect a battery to power up the kit as shown in the image below.

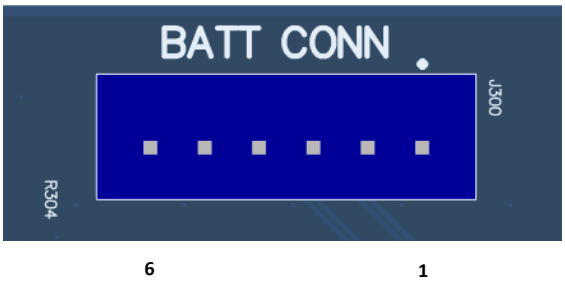


Figure 7. Battery Connector J300 (3)

Table 4. Battery Connector J300 Pinout

Pin No	Signal	Description
1	GND	System ground, Battery Negative Wire
2	GND	System ground, Battery Negative Wire
3	BATT_THERM_CONN	Thermistor
4	BATT_ID_CONN	ID Resistor
5	VBATT_CONN	Battery Positive Wire
6	VBATT_CONN	Battery Positive Wire

3.7.4 SOM Current Sense Header J301 (5)

The SOM Current Sense header, J301, can be used to monitor the SOM's current consumption on the main SOM_SYS_PWR power rail.

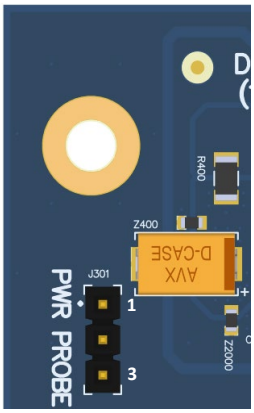


Figure 8. SOM Current Sense Header J301 (5)

The table below summarizes the pin outs of header J301

Table 5 - Power Header J301 Pinout

Pin No	Signal	Description
1	SOM_PWR_SENSE_P	SOM power positive current sense line
2	SOM_PWR_SENSE_N	SOM power negative current sense line
3	GND	System Ground

To obtain power consumption measurements, the header is connected to a data acquisition unit (Keithley 2701 or similar) and the voltages on the SOM_PWR_SENSE_P/N pins are captured a few times a second over the test period (typically 30 minutes). The SOM power consumption is then calculated as (where Rsense = 5 milliohms):

$$Psom = Vsom_{pwr_{sense_N}} * \frac{(Vsom_{pwr_{sense_P}} - Vsom_{pwr_{sense_N}})}{Rsense}$$

Use averaging to reduce noise.

3.7.5 Coin Cell Battery Holder B300 (37)

The coin cell holder allows the user to use a coin cell for supplying power to the SOM VCOIN power input. It is recommended that the Panasonic ML621 series rechargeable coin cell be used (not supplied with the development kit).

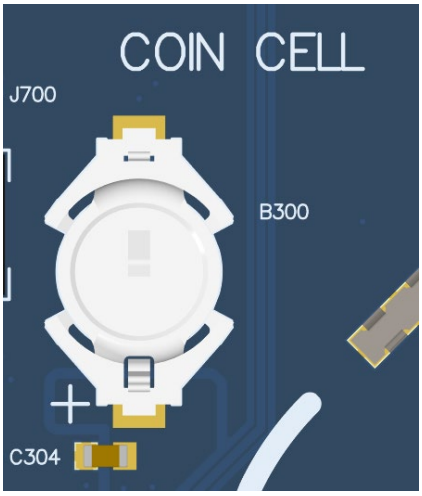


Figure 9. Coin Cell Battery Holder B300

3.7.6 Power Header J700 (36)

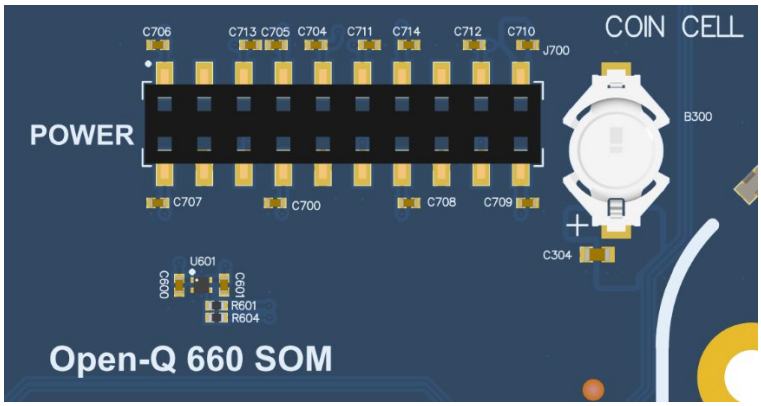


Figure 10. Power Header J700 (36)

The Power Header J700 provides main carrier board switching rails – 1.8V, 3.3V, 5.0V and 12V as well as a few carrier board LDO regulators for custom camera modules or any other purposes supplying 1.1V and 2.8V low noise power. The pinout of the connector is listed in next table.

Table 6. Power Header J700 (36)

Pin No	Signal	Description	Pin No	Signal	Description
1	MB_ELDO_CAM0_DVDD_1P1	+1.1V Carrier Board LDO for CAM 0 DVDD, Camera core	2	MB_ELDO_CAM0_VCM_2P8	+2.8V Carrier Board LDO for CAM 0 VCM
3	No Net	NC	4	GND	System Ground
5	MB_VREG_1P8	+1.8V Carrier Board Buck Power Supply for general +1.8V rail	6	MB_VREG_3P3	+3.3V Carrier Board buck-boost power supply for general +3.3V rail
7	MB_ELDO_CAM1_DVDD_1P1	+1.1V Carrier Board LDO for CAM 1 DVDD, Camera core	8	MB_ELDO_CAM0_VCM_2P8	+2.8V Carrier Board LDO for CAM 0 VCM
9	MB_ELDO_CAM1_VCM_2P8	+2.8V Carrier Board LDO for CAM 1 VCM	10	GND	System Ground
11	MB_VREG_1P8	+1.8V Carrier Board Buck Power Supply for general +1.8V rail	12	MB_VREG_3P3	+3.3V Carrier Board buck-boost power supply for general +3.3V rail
13	MB_ELDO_CAM2_DVDD_1P1	+1.1V Carrier Board LDO for CAM 2 DVDD, Camera core	14	MB_ELDO_CAM2_VCM_2P8	+2.8V Carrier Board LDO for CAM 2 VCM
15	No Net	NC	16	GND	System Ground
17	MB_VREG_1P8	+1.8V Carrier Board Buck Power Supply for general +1.8V rail	18	MB_VREG_3P3	+3.3V Carrier Board buck-boost power supply for general +3.3V rail
19	MB_VREG_5P0	+5.0V Carrier Board Boost Power Supply for general +5.0V rail.	20	DC_IN_12V	Main +12.0V Power from DC power jack

3.7.7 User Buttons and LEDs

There are four user buttons and four LED's on the Open-Q 660 µSOM Development Kit. Following is the information regarding the User Buttons:

Table 7. Development Kit Buttons

Reference Designator	User Button	Function
S2500 (27)	Volume +	Use this button to control or increase the volume.
S2502 (28)	Volume -/Reset	Use this button to control or decrease the volume. This button can also be used to reset the board.
S2501 (29)	GP Switch	This is a general-purpose user button.
S2503 (26)	Power ON	Use this button to power on the Open-Q 660 development kit.

Following is the information regarding the User LED's:

Table 8. Development Kit LEDs (24)

Reference Designator	LED	Function
DS2500	Blue LED	General purpose LED
DS2501	Green LED	General purpose LED
DS2502	Red LED	General purpose LED
DS2503	Green LED	LED indicates input power
DS2504	Red LED	LED indicates charging state

3.7.8 Debug Serial UART over USB J1600 (12)

Figure 11. Debug UART over USB J1600

The UART connection used on the Open-Q 660 is a USB micro B connector (J1600). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed. Use latest FTDI drivers from https://www.ftdichip.com/FTDrivers.htm instead of system update.

3.7.9 USB Type C (for ADB) J2300 (11)

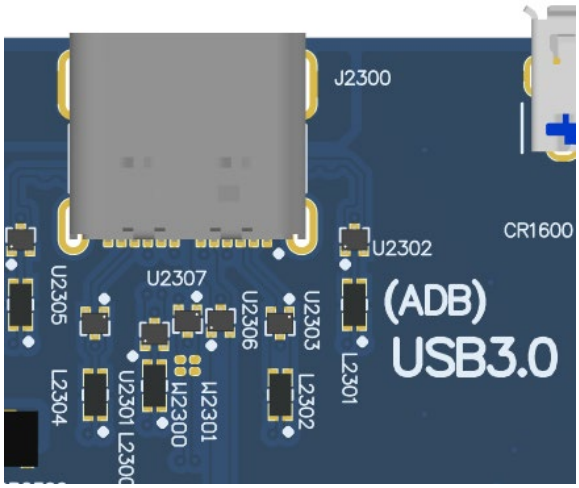


Figure 12. USB Type C (for ADB) J2300

The USB connection on the Open-Q 660 is a USB Type C connector (J2300). This connection is used for Android debug bridge (ADB) functionality. To get the adb shell, ensure that the board is up and running and connect the Type C cable between the board and the PC. Type the command adb root and adb shell on the PC prompt to exercise the adb shell functionality. While ADB utilizes only the high speed channel, this USB type C connector supports the USB 3.0 specification including the super speed data channel.

3.7.10 USB 2.0 Type A Connector J2400 (6)

The Open-Q 660 carrier board contains one USB Type A connector J2400 situated on the north side of carrier board, which exposes USB 2.0 host functionality. The standard USB 2.0 connector provides 500mA VBUS current capability for external devices.

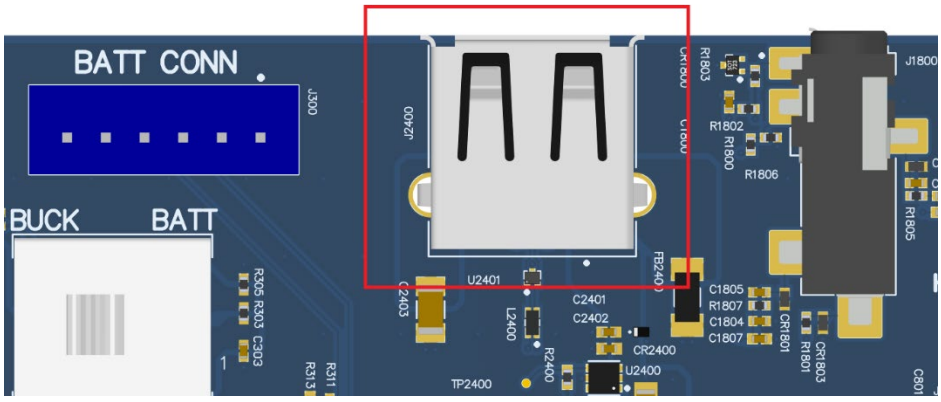


Figure 13. USB 2.0 Type A Connector J2400 (6)

3.7.11 Micro SD Card Socket J1500 (34)

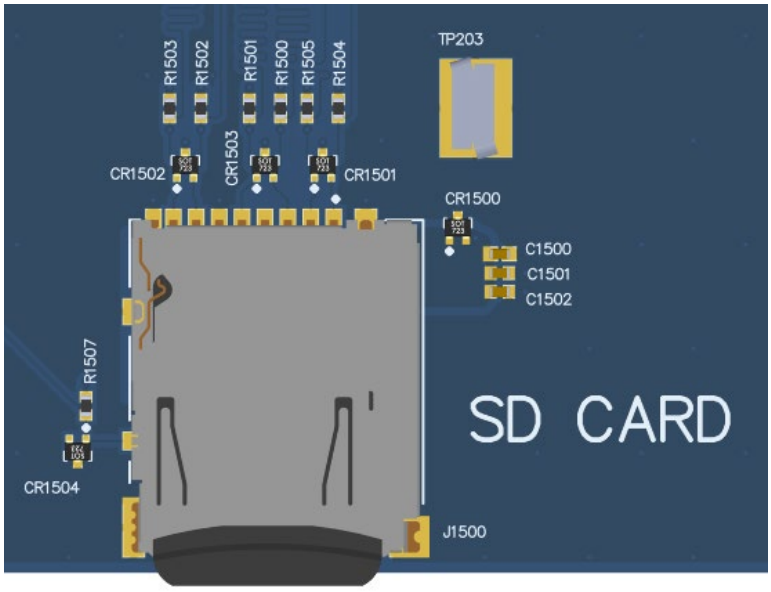


Figure 14. Micro SD Card Socket J1500

J1500 (Micro-SD card connector) provides 4-bit secure digital (SD) interface for external storage. It is located on the bottom side of the carrier board right under the Display Module. The SD interface supports High Speed mode.

3.7.12 Display Connector J1300 (30)

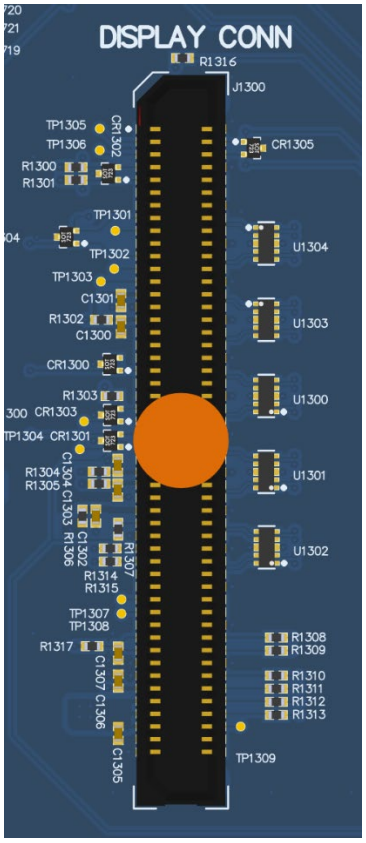


Figure 15. Display Connector J1300

The 100-pin display connector, J1300, allows for an optional display adapter to be connected to the development kit. Lantronix offers a compatible LCD panel accessory for the Open-Q 660 µSOM Development Kit. It can be purchased here: https://shop.intrinsyc.com/products/open-q-810-820-lcd.

Exposed on the display connector are the following interfaces:

- Two 4-lane MIPI DSI high speed display interfaces
- LCD backlight control signals
- I2C bus for touch panel support
- Additional GPIOs for general purposes available
- Various power rails for powering the display adapter

For details on the signal list provided on the display connector, see the development kit schematic (R-3) and the display adapter design guide technical note document (R-4).

3.7.13 Camera Connectors J1000 (15), J1100 (16), J1200 (17)

The Open-Q 660 µSOM Development Kit includes three camera interface connectors, J1000, J1100 and J1200 allowing users to connect multiple camera adapters to the development kit. Lantronix offers compatible camera module accessories for the Open-Q 660 µSOM Development Kit here: https://shop.intrinsyc.com/collections/accessories.

Exposed on each camera connector are the following interfaces:

- One 4-lane MIPI CSI high speed camera interface
- I2C bus for camera and actuator control
- Additional GPIOs for general purposes available
- Various power rails for powering the camera adapter

The three camera interfaces are almost identical. For details on the signal list provided on the camera connectors, see the development kit schematic (R-3) and the camera adapter design guide technical note document (R-5).

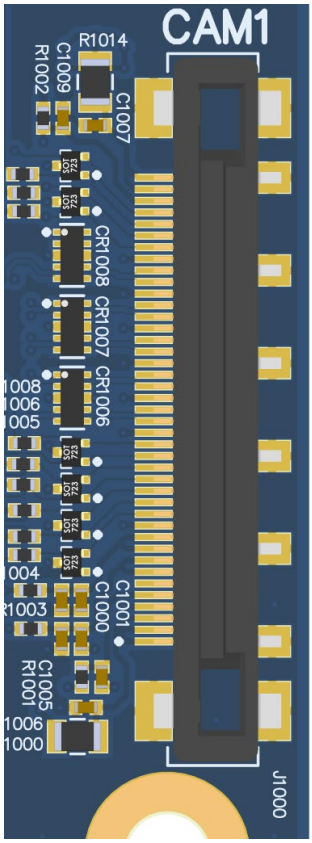


Figure 16. Typical Camera Connector

3.7.14 Camera Flash/Torch Connectors J1001 (18) and J1201 (19)

In addition to the three camera connectors, the video capturing subsystem of the Open-Q 660 µSOM Development Kit is equipped with two connectors for flash or torch devices (J1001 and J1201). The power management IC PM660 has three flash channels, each with a maximum 1.5A rated regulated current sink. However, the development kit exposes only two of the flash channels with a 0.25A current limit, due to current limit of SOM connectors pins.

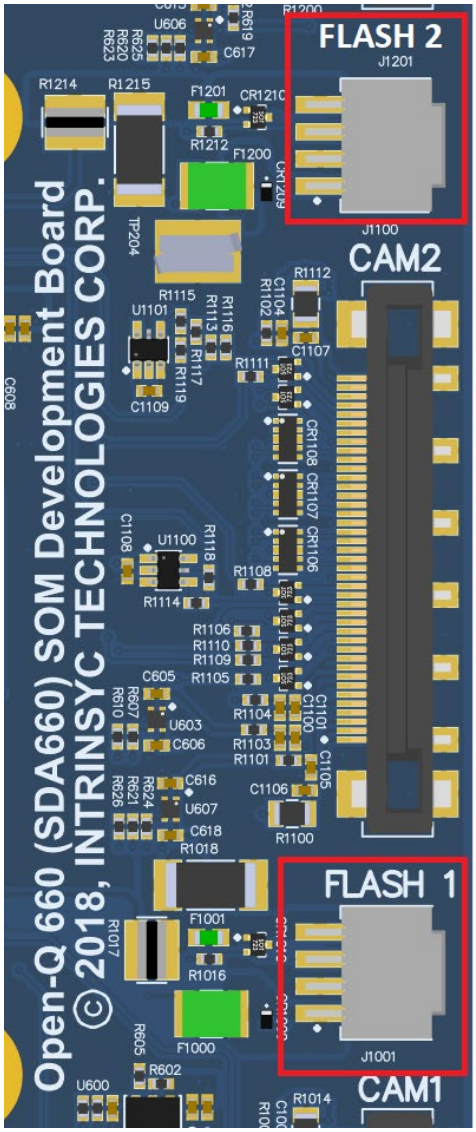
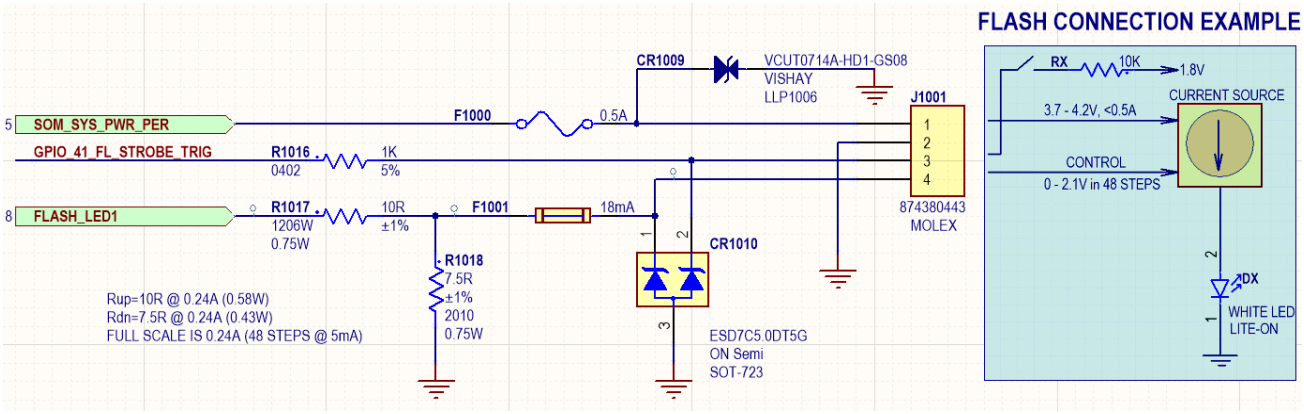


Figure 17. Camera Flash/Torch Connectors J1001 (18) and J1201 (19)

Table 9. Camera Flash/Torch Connectors pinout

Pin No	Signal Name	Description
1	SOM_SYS_PWR_PER	System power 3.9V. Current limited to <0.5A
2	GND	System ground
3	GPIO_41_FL_STROBE_TRIG	APQ GPIO 41, input from external CMOS level flash trigger
4	FLASH_LED1 or FLASH_LED2	PM660 flash current sink channel 1 and 2, Full scale 0.24A regulated in 48 steps

Typical interfacing to these flash channels is shown below:



3.7.15 Digital IO Expansion Header J2200 (31)

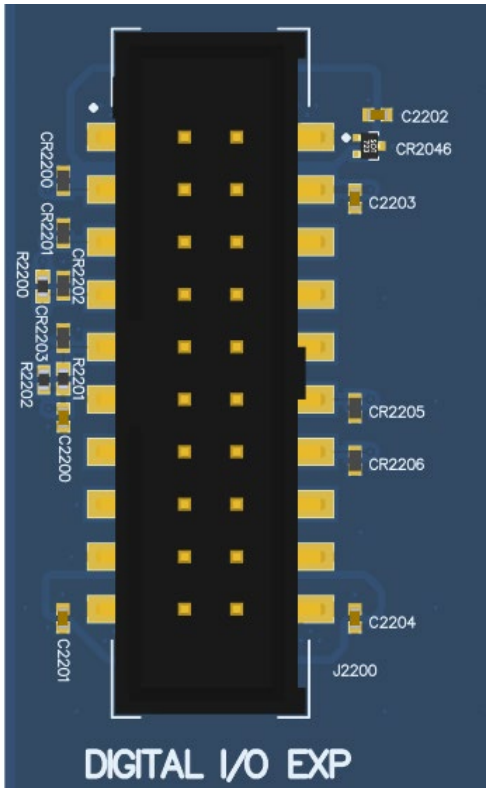


Figure 18. Digital IO Expansion header J2200

The header J2200 is a 20-pin connector that provides access to a selection of SOM GPIO signals and power rails. The following table shows the pin out description for this header.

Table 10. Digital IO Expansion Header J2200 Pinout

Pin No	Signal	Description	Pin No	Signal	Description
1	VREG_L13A_1P8	PMIC LDO Regulator L13A. 1.8V	2	VREG_L13A_1P8	PMIC LDO Regulator L13A. 1.8V
3	GPIO_0_BLSP1_SPI_MOSI	APQ BLSP1 SPI, GPIO_0. Master output	4	MB_VREG_3P3	Carrier board switching regulator. 3.3V
5	GPIO_1_BLSP1_SPI_MISO	APQ BLSP1 SPI, GPIO_1. Master input	6	No Net	
7	GPIO_2_BLSP1_SPI_CS_N	APQ BLSP1 SPI, GPIO_2. Chip Select	8	No Net	
9	GPIO_3_BLSP1_SPI_CLK	APQ BLSP1 SPI, GPIO_3. Clock	10	No Net	
11	GND	Ground	12	LPI_GPIO_14_UART_2_TX	Low Power APQ GPIO_14, UART TX
13	No Net		14	LPI_GPIO_15_UART_2_RX	Low Power APQ GPIO_15, UART RX
15	No Net		16	No Net	
17	GND	Ground	18	GND	Ground
19	MB_VREG_5P0	Carrier board switching regulator. 5.0V	20	MB_VREG_5P0	Carrier board switching regulator. 5.0V

For more details regarding configuring the GPIOs on this header, refer to the Open-Q 660 Software Release Notes to determine feature support in the latest software release.

3.7.16 Sensor IO Expansion Header J2100 (25)

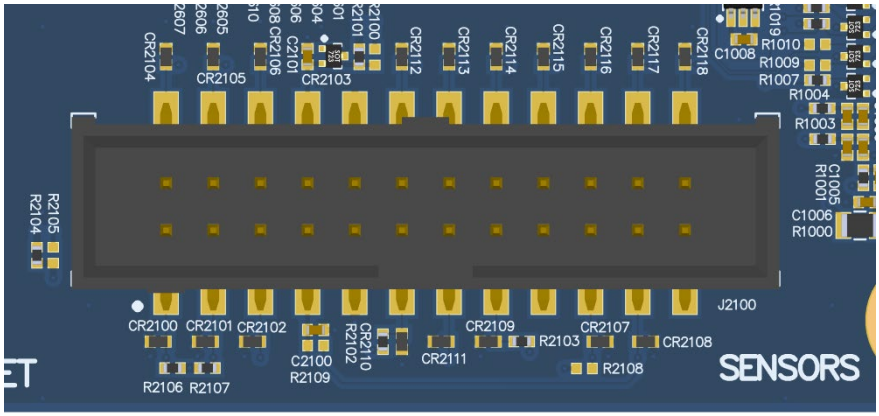


Figure 19. Sensor Expansion Header J2100

The sensor expansion header J2100 allows for a 24-pin connection to an optional sensor board. If user application does not require a sensor, then this header can be used for other applications that require I2C, SPI or GPIO input and output connections. Following is the pin breakout for sensor expansion header J2100.

Table 11 - Sensor Expansion Header J2100 Pinout

Pin No	Signal	Description	Pin No	Signal	Description
1	LPI_GPIO_2_I2C_3_SDA	APQ GPIO 2, I2C 3, Data	2	GPIO_68_ACCEL_INT	APQ GPIO 68
3	LPI_GPIO_3_I2C_3_SCL	APQ GPIO 2, I2C 3, Clock	4	GPIO_74_CAP_INT_N	APQ GPIO 74
5	GPIO_42_MEMS_RESET_N	APQ GPIO 42	6	GPIO_69_GYRO_INT	APQ GPIO 68
7	VREG_L14A_SNS_1P8	PMIC LDO Regulator L14A. 1.8V	8	SENS_ANA_PWR	PMIC LDO Regulator L3B. 3V0
9	GND	Ground	10	GND	Ground
11	GPIO_73_HRM_INT	APQ GPIO 73	12	GPIO_72_FP_INT_N	APQ GPIO 72
13	LPI_GPIO_0_SPI_1_CS1_N	Low Power APQ GPIO 0, SPI1 Chip Select Neg.	14	GPIO_71_ALSPG_INT_N	APQ GPIO 71
15	GPIO_21_SNS_GP1	APQ GPIO 21	16	GPIO_70_MAG_INT_N	APQ GPIO 70
17	No Net		18	GPIO_75_HALL_INT_N	APQ GPIO 75

19	LPI_GPIO_8_SPI_1_CS_N	Low Power APQ GPIO 8, SPI1 Chip Select Neg.	20	LPI_GPIO_10_SPI_1_MOSI	Low Power APQ GPIO 10, SPI1 Master Output
21	LPI_GPIO_9_SPI_1_CLK	Low Power APQ GPIO 9, SPI1 Clock	22	LPI_GPIO_11_SPI_1_MISO	Low Power APQ GPIO 11, SPI1 Master Input
23	No Net		24	LPI_GPIO_1_PWR_EN	Low Power APQ GPIO 1, Power Enable

Please refer to the schematic and consider the power before connecting anything to this header. For more details regarding configuration, refer to the Open-Q 660 Software Release Notes to determine feature support in the latest software release.

3.7.17 Audio Inputs Expansion Header J1900 (33)

The Open-Q 660 µSOM Development Kit Audio subsystem is built around the Qualcomm Audio Codec WCD9335. There are a few headers that expose capabilities of WCD9335 for the user. The Audio Inputs Expansion Header J1900 (33) provides signals to handle up to six microphones.

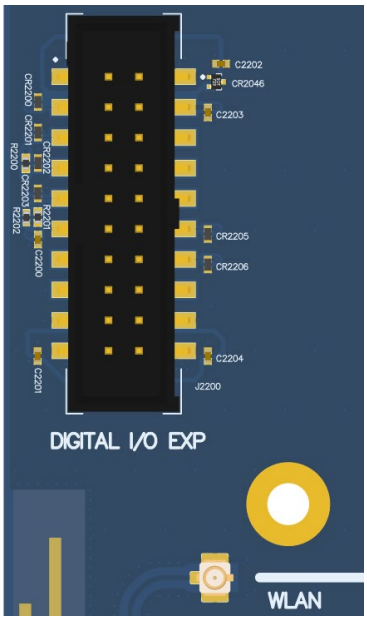


Figure 20. Audio Inputs Expansion Header J1900 (33)

Table 12. Audio Inputs Expansion Header Pinout J1900 (33)

Pin No	Signal	Description	Pin No	Signal	Description
1	CDC_IN1_P	Codec Input 1 Positive	2	CDC_IN1_N	Codec Input 1 Negative
3	CDC_IN5_P	Codec Input 5 Positive	4	CDC_IN5_N	Codec Input 5 Negative
5	CDC_MIC_BIAS1	Microphone Bias 1	6	CDC_MIC_BIAS3	Microphone Bias 3
7	CDC_IN6_P	Codec Input 6 Positive	8	CDC_IN6_N	Codec Input 6 Negative
9	CDC_MIC_BIAS4	Microphone Bias 4	10	MB_VREG_3P3	3.3V Carrier board Switching Regulator
11	GND	System Ground	12	GND	System Ground
13	CDC_DMIC_CLK0	Digital Microphone 0 Clock	14	CDC_DMIC_CLK1	Digital Microphone 1 Clock
15	CDC_DMIC_DATA 0	Digital Microphone 0 Data	16	CDC_DMIC_DATA 1	Digital Microphone 1 Data
17	MB_VREG_1P8	1.8V Carrier board Switching Regulator	18	CDC_DMIC_CLK2	Digital Microphone 2 Clock
19	GND	System Ground	20	CDC_DMIC_DATA 2	Digital Microphone 2 Data

3.7.18 Audio Outputs Expansion Header J1901 (32)

The Audio Outputs Expansion Header J1901 (32) provides two differential and two single ended line outputs, earpiece amplifier, one codec PDM 1-bit interface, and some GPIO signals to implement any required custom logic. The carrier board rails 1.8V, 3.3V, 5.0V and 12V are also exposed. The connector pinout is shown in next table.

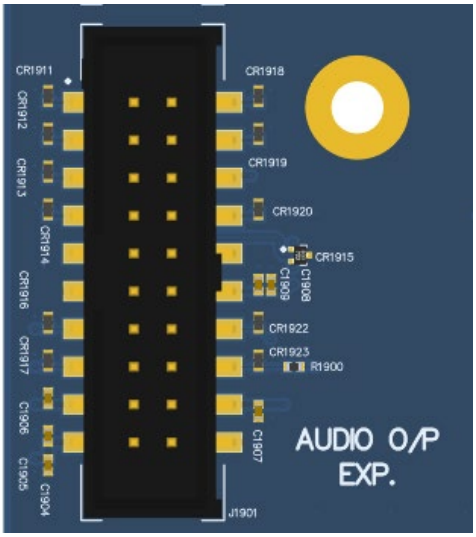


Figure 21. Audio Outputs Expansion Header J1901 (32)

Table 13. Audio Outputs Expansion Header Pinout J1901

Pin No	Signal	Description	Pin No	Signal	Description
1	CDC_LINE_OUT1_P	Codec Line Out 1 Positive	2	CDC_LINE_OUT1_N	Codec Line Out 1 Negative
3	CDC_LINE_OUT2_P	Codec Line Out 2 Positive	4	CDC_LINE_OUT2_N	Codec Line Out 2 Negative
5	CDC_LINE_REF	Codec Reference	6	MB_VREG_3P3	3.3V Carrier Board Switching Regulator
7	CDC_LINE_OUT3	Codec Line Output 3	8	CDC_LINE_OUT4	Codec Line Output 4
9	CDC_EAR_P	Earphone Amplifier Output Positive	10	CDC_EAR_N	Earphone Amplifier Output Negative
11	GND	System Ground	12	SOM_SYS_PWR_PER	SOM System Power
13	CDC_SWR_CLK	Codec PDM Clock	14	CDC_SWR_DATA	Codec PDM Data
15	GPIO_80_SPKR_AMP_EN1	GPIO, can be Speaker Amplifier Enable 1	16	AMP_EN2	GPIO77, can be Speaker Amplifier Enable 2
17	MB_VREG_1P8	1.8V Carrier Board Switching Regulator	18	DC_IN_12V	Main 12.0V Power

Pin No	Signal	Description	Pin No	Signal	Description
19	MB_VREG_5P0	5.0V Carrier Board Switching Regulator	20	GND	System Ground

3.7.19 Audio IO Expansion Headers 1 and 2, J2000 (9) and J2001 (7)

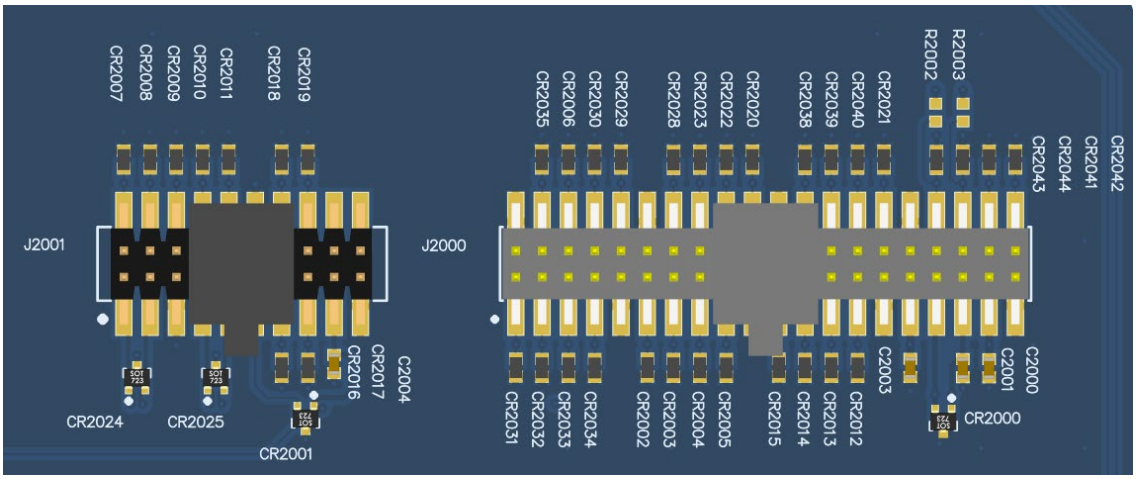


Figure 22. Audio IO Expansion Headers 1 and 2, J2000 and J2001

The Audio IO expansion headers J2000 and J2100 are 40-pin and 20-pin connecters that expose digital audio related signals as described in the pinout table below.

Table 14. Audio IO Expansion Header #1 J2000 Pinout

Pin No	Signal	Description	Pin No	Signal	Description
1	GPIO_8_BLSP3_SPI_MOSI	APQ BLSP3, GPIO 8, SPI Master Output	2	GND	Ground
3	GPIO_9_BLSP3_SPI_MISO	APQ BLSP3, GPIO 9, SPI Master Input	4	PM660_GPIO_3_DIV_CLK_1_R_IO	PMIC GPIO 3, Clock output
5	GPIO_10_BLSP3_SPI_CS_N	APQ BLSP3, GPIO 10, SPI Chip Select Neg	6	GPIO_61_MI2S_1_MCLK	APQ GPIO 61, MI2S 1, Master Clock
7	GPIO_11_BLSP3_SPI_CLK_N	APQ BLSP3, GPIO 11, SPI Clock	8	LPI_GPIO_23_AUD_CDC_INT2_CON	Low Power APQ GPIO 23, Codec Interrupt 2
9	GND	Ground	10	LPI_GPIO_22_AUD_CDC_INT1_CON	Low Power APQ GPIO 23, Codec Interrupt 1
11	GPIO_12_MI2S_1_SCK	APQ GPIO 12, MI2S 1, Bit Clock	12	GND	Ground
13	GPIO_13_MI2S_1_WS	APQ GPIO 13, MI2S 1, Word Select	14	LPI_GPIO_21_AUD_SB_DATA1_CON	Low Power APQ GPIO 20, Sound Bus Data 1
15	GPIO_14_MI2S_1_D0	APQ GPIO 14, MI2S 1, Data 0	16	LPI_GPIO_20_AUD_SB_DATA0_CON	Low Power APQ GPIO 20, Sound Bus Data 0
17	GPIO_15_MI2S_1_D1	APQ GPIO 15, MI2S 1, Data 1	18	LPI_GPIO_19_AUD_SB_CLK_CON	Low Power APQ GPIO 19, Sound Bus Clock
19	GND	Ground	20	LPI_GPIO_18_WCD_SDM_MCLK_CON	Low Power APQ GPIO 18, Master Clock
21	LPI_GPIO_7	Low Power APQ GPIO 7	22	GND	Ground
23	LPI_GPIO_6	Low Power APQ GPIO 6	24	GPIO_45_AUD_IO_EXP_1	APQ GPIO 45
25	LPI_GPIO_5	Low Power APQ GPIO 5	26	GPIO_49_AUD_IO_EXP_2	APQ GPIO 49
27	LPI_GPIO_4	Low Power APQ GPIO 4	28	GPIO_20_AMP_PWR_EN	APQ GPIO 20
29	GND	Ground	30	LPI_GPIO_17_MI2S_4_WS_CON	Low Power APQ GPIO 13, MI2S 4, Word Select
31	MB_VREG_1P8	Carrier Board Regulator, 1.8V	32	GND	Ground
33	MB_VREG_3P3	Carrier Board Regulator, 3.3V	34	GPIO_30_AUD_IO_GP1	APQ GPIO 30

35	MB_VREG_5P0	Carrier Board Regulator, 5.0V	36	GPIO_31_AUD_IO_GP 2	APQ GPIO 31
37	DC_IN_12V	Main 12.0V Power	38	GPIO_28_AMP_FAUL T	APQ GPIO 28
39	GND	Ground	40	GPIO_29_AMP_RST_ N	APQ GPIO 29

Table 15. Audio IO Expansion Header #2 J2001 Pinout

Pin No	Signal	Description	Pin No	Signal	Description
1	CDC_IN3_P	Analog Microphone Input 3, Pos	2	GPIO_62_MI2S_2_M CLK	APQ GPIO 62, MI2S 2, Master Clock
3	CDC_IN3_N	Analog Microphone Input 3, Neg	4	GPIO_24_MI2S_2_S CK	APQ GPIO 24, MI2S 2, Bit Clock
5	GND	Ground	6	GPIO_25_MI2S_2_ WS	APQ GPIO 25, MI2S 2, Word Select
7	CDC_IN4_P	Analog Microphone Input 4, Pos	8	GPIO_26_MI2S_2_D 0	APQ GPIO 26, MI2S 2, Data 0
9	CDC_IN4_N	Analog Microphone Input 4, Neg	10	GPIO_27_MI2S_2_D 1	APQ GPIO 27, MI2S 2, Data 1
11	CDC_MIC_BIAS1	Microphone Bias 1	12	GND	Ground
13	LPI_GPIO_26_DMIC 1_CLK	Digital Mic 1, PDM Clock	14	LPI_GPIO_28_DMIC 2_CLK	Digital Mic 2, PDM Clock
15	LPI_GPIO_27_DMIC 1_DATA	Digital Mic 1, PDM Data	16	LPI_GPIO_29_DMIC 2_DATA	Digital Mic 2, PDM Data
17	MB_VREG_1P8	Carrier Board Regulator, 1.8V	18	No Net	
19	GND	Ground	20	No Net	

Please refer to the schematic and consider the power before connecting anything to these headers. For more details regarding configuration, refer to the Open-Q 660 Software Release Notes to determine feature support in the latest software release.

3.7.20 Audio Headset Jack J1800 (8)

In addition to expansion headers, the user can use standard 3.5mm Audio Headset Jack J1800 directly, which provides stereo output to headphone, microphone input and headset detection circuits.

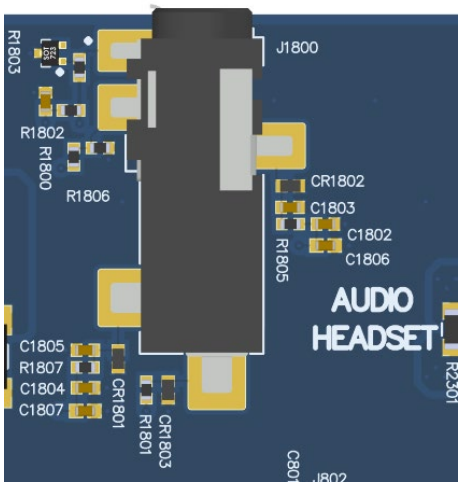


Figure 23. Audio Headset Jack J1800 (8)

3.7.21 WLAN / BT Antenna Connections

The Open-Q 660 µSOM Development Kit WLAN/BT functionality is based on Qualcomm WCN3990 chipset. It provides WLAN/Bluetooth in 2x2 MIMO with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards, and Bluetooth + LE 5.x + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.

The chipset is placed on SOM which has U.FL coax connectors for channel 0 (WLAN+BT) and channel 1 (WLAN only). These connectors are mated to the Carrier board WLAN / BT PCB antennas via coax cables. The two images below show the two channels of the WLAN / BT connections on SOM and how they are routed on carrier board.

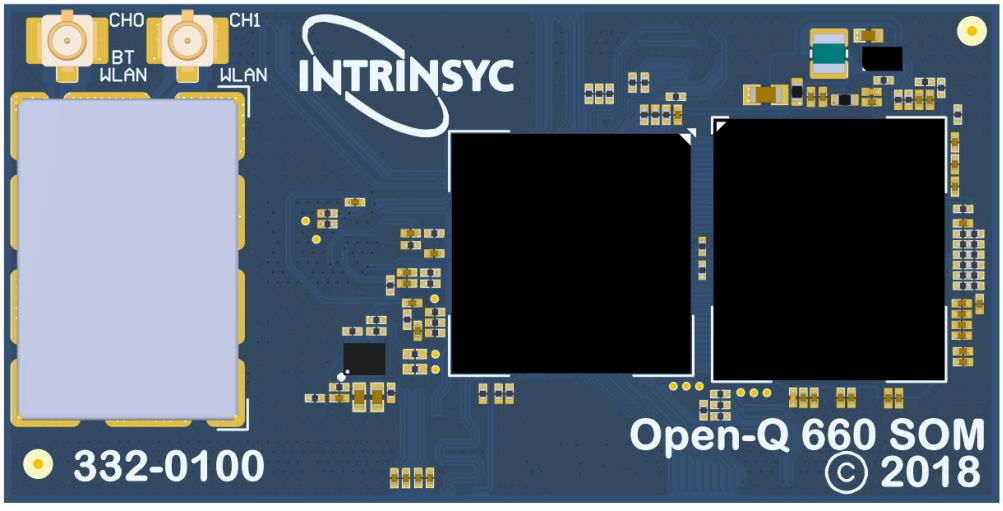


Figure 24. WLAN / BT SOM Connections (21, 22)

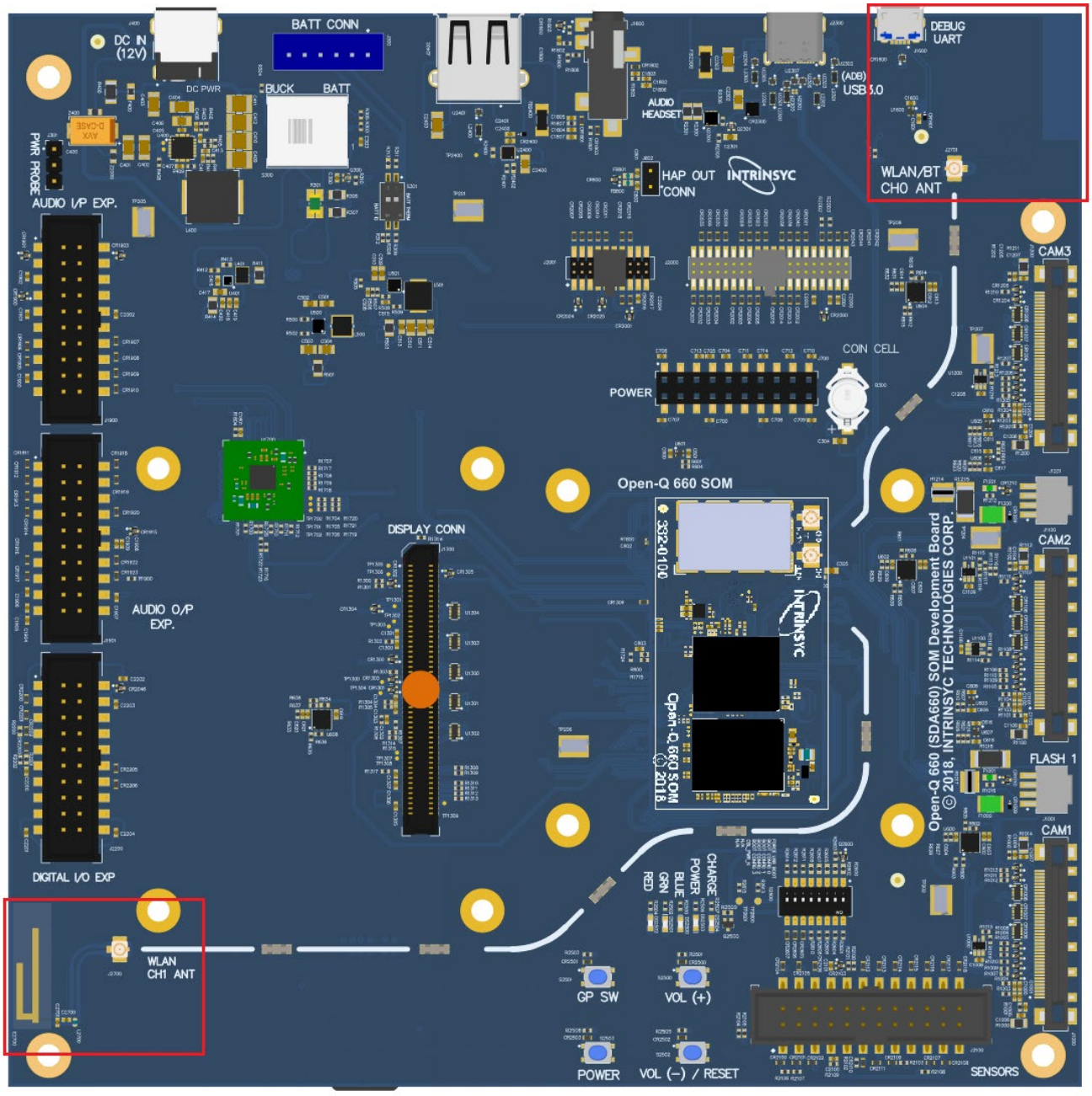


Figure 25. Channel 0 and 1 WLAN/BT routing and PCB Antennas on Carrier Board

If more advanced antenna solution is required it is always possible to connect custom antennas to the SOM U.FL connectors.

3.7.22 Quiet Thermistor RT800 (35)

The Quiet Thermistor RT800 is provided to allow better control over the system thermal management mechanism.

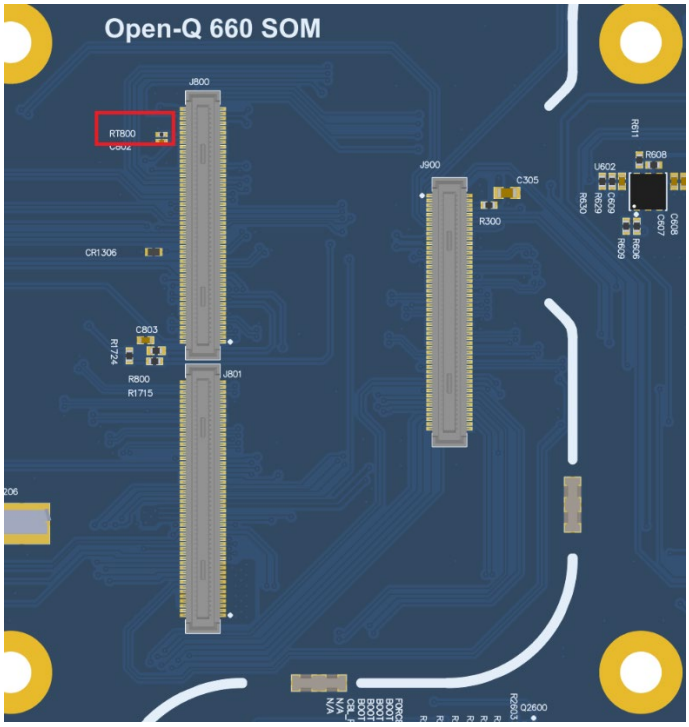


Figure 26. Quiet Thermistor RT800 Location (34)

3.7.23 Haptic Output Header J802 (10)

The haptic output header J802 is provided for the user to gain access to the SOM's PM660 haptic output driver. This driver supports both ERM and LRA modes. Pin 1 is positive and pin 2 is negative driver's lines.

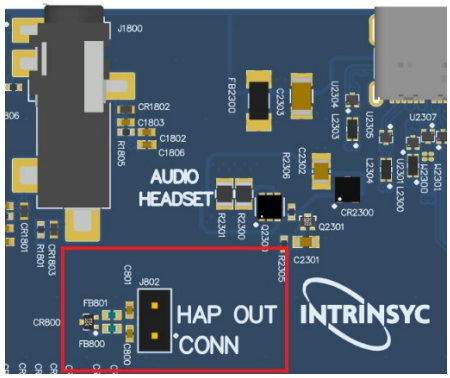


Figure 27. Haptic Output Header J802 (10)