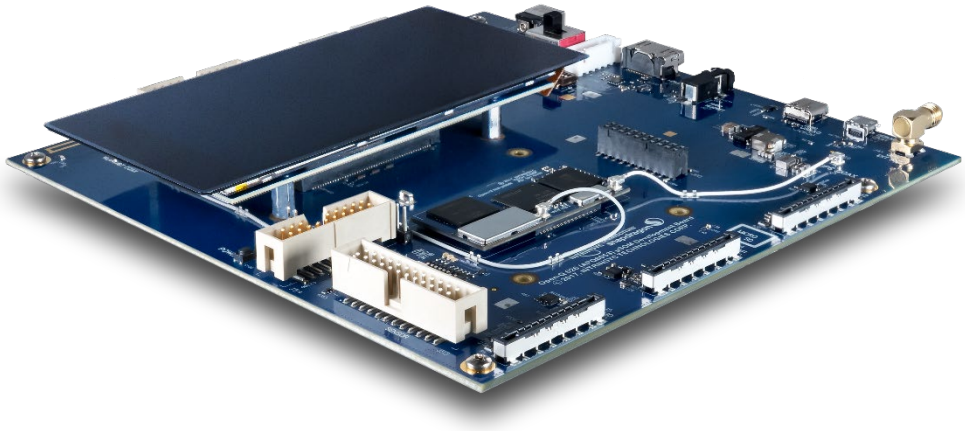
LANTRONIX® Formerly INTRINSYC



Open-Q™ 626 Development Kit User Guide

Part Number PMD-00037

Revision A August 2020

Contacts

Lantronix, Inc.
7535 Irvine Center Drive, Suite 100
Irvine, CA 92618, USA
Toll Free: 800-526-8766
Phone: 949-453-3990
Fax: 949-453-3995

IES Customer Support Portal
https://helpdesk.intrinsyc.com

Lantronix Technical Support
http://www.lantronix.com/support

Sales Offices
For a current list of our domestic and international sales offices, go to the Lantronix web site at http://www.lantronix.com/about-us/contact/

Revision History

Date	Rev.	Comments
September 2017	1.0	Initial release. Intrinsyc document number: ITC-01RND1278-UG-001
October 2017	1.1	Cleaned up typos, updated photos, added sections: • Getting Started • Battery config switches • Optional Accessories
August 2020	A	Initial Lantronix document. Added Lantronix document part number, Lantronix logo, branding, contact information, and links.

For the latest revision of this product document, please go to: http://tech.intrinsyc.com.

Contents

1 Introduction

1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q™ 626 Development Kit based on the Qualcomm™ 626 (APQ8053-Pro) Processor.

For more background information on this development kit, visit: https://www.lantronix.com/products/open-q-626-usom-development-kit/

1.2 Scope

This document will cover the following items on the Open-Q 626 Development Kit:

- Block Diagram and Overview
- Hardware Features
- Configuration
- SOM
- Carrier Board
- Display Board for LCD (Optional)

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Lantronix Open-Q 626 Development Kit.

2 Documents

This section lists the supplementary documents for the Open-Q 626 development kit.

2.1 Applicable Documents

Reference	Title
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.2 Reference Documents

Reference	Title
R-1	Open-Q 626 Schematics (SOM, Carrier)
R-2	Open-Q 626 Dev Kit SOM Tech Note

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array
GPS	Global Positioning system
HDMI	High Definition Media Interface
HSIC	High Speed Inter Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SOM	System on Module

Term and acronyms	Definition
SPMI	System Power Management Interface (Qualcomm® PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm® proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

2.4 List of Figures

2.5 List of Tables

3 Open-Q 626 Development Kit

3.1 Introduction

The Open-Q 626 provides a quick reference or evaluation platform for Qualcomm's 626 chipset. This kit is suited for Android / Linux application developers, OEMs, consumer manufacturers, hardware component vendors, video surveillance, robotics, camera vendors, and flash chip vendors to evaluate, optimize, test and deploy applications that can utilize the Qualcomm® 626 series technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 626 Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

3.4 Kit Contents

The Open-Q 626 Development Kit includes the following:

- Open-Q 626 System on Module (SOM) with the Qualcomm APQ8053-Pro processor
- Open-Q 626 Mini-ITX form-factor carrier board
- 4.5" FWVGA (480x854) 16.7 M LCD (optional accessory)
- AC power adapter
- HDMI cable.

See the diagram and list below for locations of the key components, interfaces, and controls.

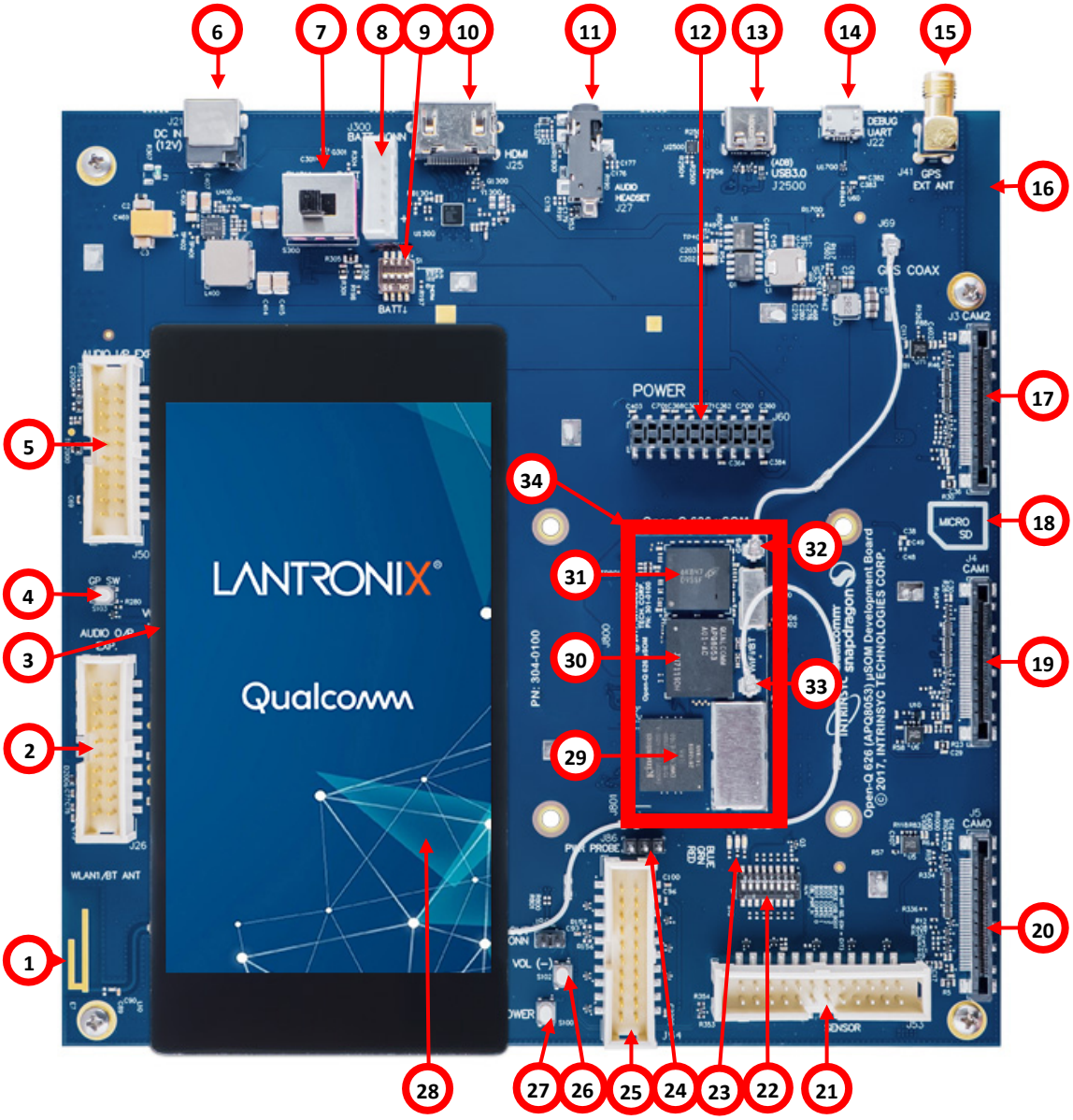


Figure 1 Open-Q 626 Development Kit

List of features highlighted in above photo:

1. WLAN PCB Antenna
2. Audio output expansion header
3. Volume + button
4. General Purpose button
5. Audio input expansion header
6. 12V DC input jack

7. Power source switch
8. Battery connector
9. Battery charge config switch
10. HDMI video output
11. 3.5 mm headset jack
12. Power header
13. USB Type-C connector
14. Debug UART (USB MicroB)
15. GPS ext. ant. SMA connector
16. GPS PCB Antenna (on bottom)
17. MIPI camera 2 connector
18. Micro SD slot (on bottom)
19. MIPI camera 1 connector
20. MIPI camera 0 connector
21. Sensor board header
22. Configuration DIP switches
23. 3 x LEDs
24. SOM power measurement header
25. GPIO expansion header
26. Volume - button
27. Power button
28. MIPI DSI LCD/touchscreen connector to interface with LAntronix display adapter
29. 16GB eMMC flash memory
30. APQ8053 CPU
31. 2GB LPDDR3 RAM memory
32. GPS antenna connector U.FL
33. WLAN antenna connector U.FL
34. Open-Q 626 System on Module (SOM)

3.5 Software

The development kit comes with Android software pre-programmed on the SOM. Please see the Lantronix support site for further information about the software like Release Notes, Programmer's Guide and other available software versions. The support site is at: http://tech.intrinsyc.com and registration of your development kit is required.

The software version number can be checked in the "Android settings -> About Phone -> Build Number", and cross-referenced with the release notes to confirm which features are supported and what known issues there are with the specific software release you have.

To register your development kit, please visit: https://tech.intrinsyc.com/account/register and you will require the serial number from the SOM as described in the next section.

3.6 Hardware Identification Label

Labels are present on the SOM and the carrier board. The following information is conveyed on these two boards:

SOM: Serial number, WIFI MAC address

Carrier board: Serial number

Note: Please retain the SOM and carrier board serial numbers for warranty purposes.

Refer to http://tech.intrinsyc.com/projects/serialnumber/wiki for more details about locating the serial number, as this is needed to register your development kit on the Lantronix support site.

3.7 Optional Accessories

1. LCD / Touchscreen
2. 13MP Camera module

Please see the Lantronix website/store or contact Lantronix for availability of camera modules, sensor boards, and other accessories:

www.shop.intrinsyc.com

sales@lantronix.com

3.8 Getting Started with the Development Kit

This section explains how to set up the Open-Q 626 Development Kit and start using it.

3.8.1 Configuration Switch Settings

1. S10 DIP switches - The configuration DIP switches (S10) are by default in the OFF position and this is the correct position for normal boot and operation. For more details about the configuration switch settings see section 3.9.1.
2. S300 power switch – this switch should be set to the “BUCK” position to operate the board from the 12V power input. To operate from battery power, see sections 3.11.2 and 3.11.5 for more details.
3. S1 battery configuration DIP switch – All S1 DIP switches are ON by default and should be left in that position for normal operation from the 12V power input.

3.8.2 Powering up the Open-Q 626 Development Kit

To power-up the board, perform the following steps below:

1. At a static-safe workstation, remove the development kit board carefully from the anti-static bag.
2. If not using the optional LCD display, connect the HDMI output from the development kit to an HDMI monitor.
3. Connect the Power Adapter to the 12V DC Jack and then press and hold the power button until you see the Lantronix logo appear on the display (~3 seconds).
4. If using an HDMI monitor then plug a USB mouse into the USB Type-C connector to navigate the UI on the HDMI display.
5. If using the optional LCD display you can navigate using the touchscreen on the display.

3.8.3 Display Options

The Open-Q 626 Development Kit can be used with either the optional LCD touch panel, which mounts onto the carrier board, or with an external HDMI monitor. The LCD functions as the Android primary display and the HDMI is the secondary display and mirrors the primary. This is the default setting and no configuration change is required to use either display. The HDMI output can be used with or without the LCD panel installed.

3.9 Development Kit Block Diagram

The Open-Q 626 development platform consists of the Open-Q 626 SOM and the Carrier Board. The following block diagram shows the interconnectivity and peripherals on the development kit.

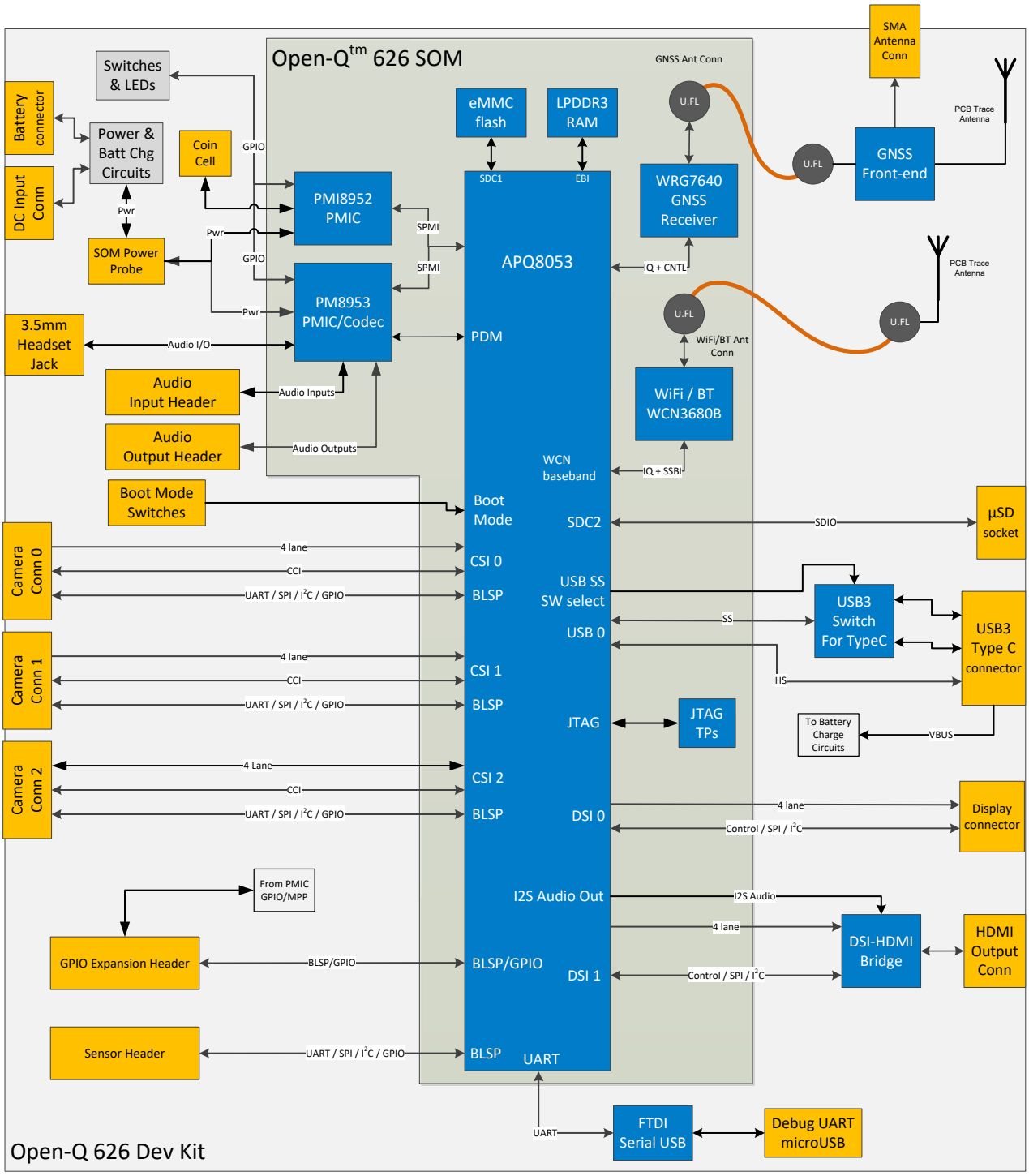


Figure 2 Open-Q 626 + Carrier Board Block Diagram

3.10 Open-Q 626 SOM

This section describes some details of the SOM. The SOM provides the basic common set of features with minimal integration efforts for end users.

It contains the following:

- Qualcomm 626 (APQ8053-Pro) main application processor
- LPDDR3 up to 933MHz (1866Mbps) 2GB RAM
- PMI8952 + PM8953 – power management, battery charging, regulators, audio codec, housekeeping
- WCN3680B Wi-Fi + BT combo chip
- 16GB eMMC v5.0 Flash Memory.
- WGR7640 GPS Receiver Front End

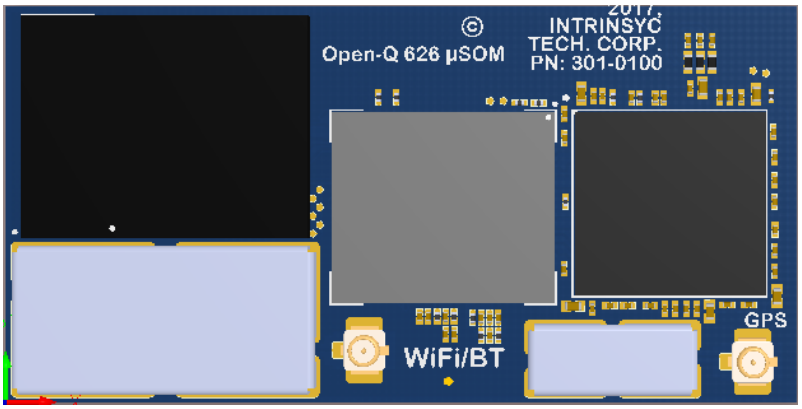


Figure 3 Open-Q 626 SOM

3.10.1 SOM Mechanical Properties

Size	50 mm x 25 mm (12.5 cm^2)
Interface	3 x 100-pins Hirose DF40 connectors (B2B Connector).
Shielding	Top side shields for the WiFi/BT & GPS front ends are installed by default.

3.10.2 SOM Block Diagram

The Open-Q 626 SOM measuring 50mm x 25mm is where all the processing occurs. It is connected to the carrier board via three 100 pin Hirose DF40 connectors. The purpose of these connectors is to bring out essential signals such that other peripherals can be connected to the platform.

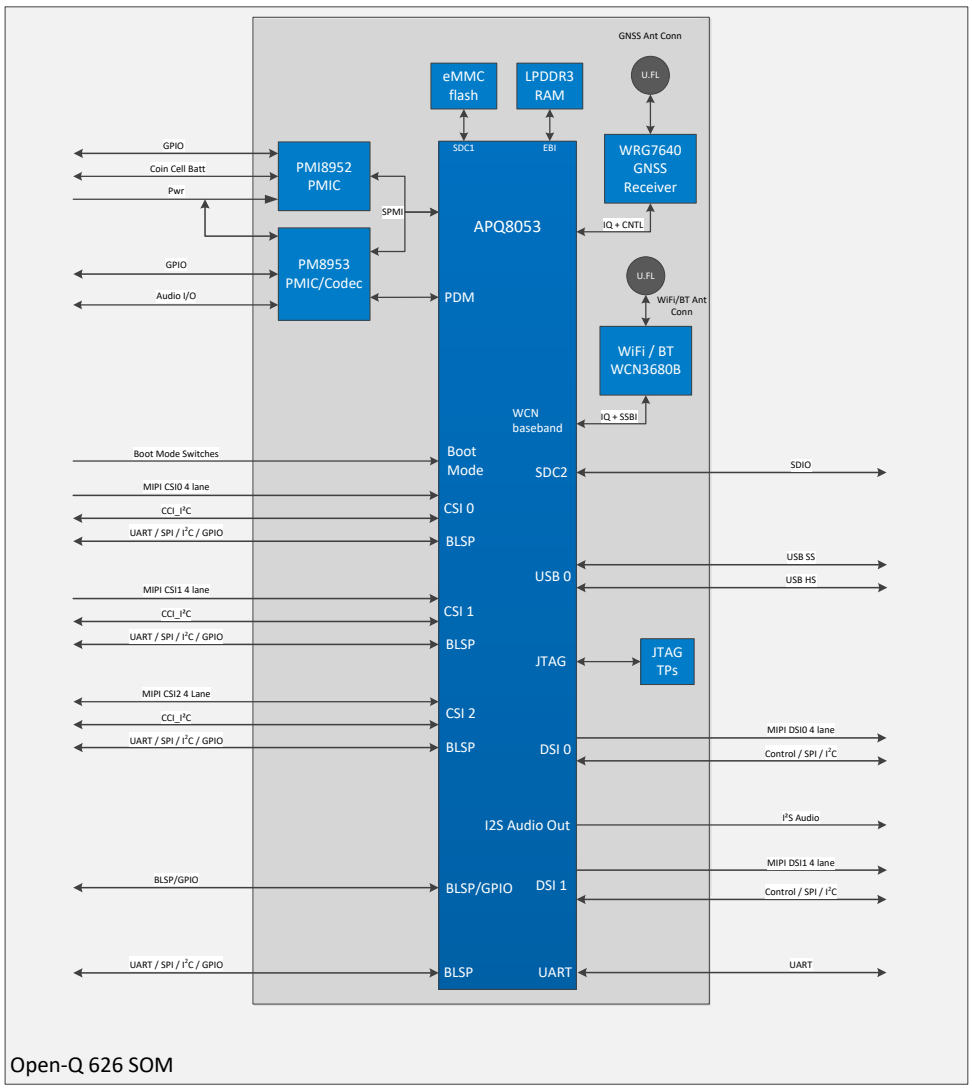


Figure 4 SOM Block Diagram

3.10.3 Hardware Specification

The Open-Q 626 platform has the following hardware features:

Table 3.1 Open-Q 626 Development Kit Hardware Features

Subsystem / Connectors	Feature Set	Description	Specification
Chipset	APQ8053-Pro	Qualcomm® 626 Processor	Octa-core, 64-bit ARM Cortex-A53 up to 2.2GHz. Adreno 506 GPU

Subsystem / Connectors	Feature Set	Description	Specification
			Hexagon 546 DSP
	PMIC (PM8953 & PMI8952)	Qualcomm® PMIC, companion power management chips for APQ8053-Pro processor	NA
Memory	2GB LPDDR3	DDR3 Low Power Memory	Up to 1866MHz LPDDR3 BGA chip. Supports via 4x16bit channels
	16 GB eMMC	Primary Storage for platform. Mainly used for storing SW applications and user data etc.	eMMC v5.0 on board.
Connectivity	Wi-Fi 2.4 GHz/ 5GHz	Qualcomm WCN3680B Wi-Fi + BT Combo Chip	802.11a/b/g/n/ac 2.4/5.0 GHz 1X1
	BT 2.4 GHz	Qualcomm WCN3680B Wi-Fi + BT Combo Chip	Supports BT 4.2 + BR/EDR + BLE.
	GPS via WGR7640	GPS Frontend	GPS, GLONASS, COMPASS
RF Interfaces	1x WLAN / BT	Connect to antenna on carrier board via coax cable	2.4/ 5 GHz
	1x GPS	Connect to antenna on carrier board via coax cable	GPS/GLONASS/COMPASS
Interfaces	3x MIPI CSI	Camera Connectors CSI0, CSI1, CSI2	MIPI Alliance Specification v1.0
	1x USB 3.0 HS/SS	1 x USB Type C receptacle with USB 3.0/2.0	USB3.0/2.0
	1x MIPI DSI (DSI0 & DSI1) + Touch 100-pin display Connector	100- pin display connector. Interfaces with Lantronix Display Adapter Board	MIPI Alliance Specification v1.01. MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01
	1x HDMI output	HDMI transmitter output video and embedded 2-channel audio	148.5 MHz maximum TMDS output clock frequency

Subsystem / Connectors	Feature Set	Description	Specification
			supports video resolutions up to 1080p at 60Hz. 2-channel audio up to 192kHz
	1x µSD Socket	Accepts µSD memory card. Push-push type socket.	SDIO Card Specification version 3.0. Secure Digital: Physical Layer Specification version 3.0.
	1x 3.5mm Headset Jack	4 conductor jack	Stereo audio output and mono microphone input
	2x Audio I/O Headers	1x Header for audio input expansion: 2x10 pin, 0.1in 1x Header for audio output expansion: 2x10 pin, 0.1in	1x Header for audio input expansion: 2x analog microphone and 1x digital microphone, and Power. 1x Header for audio output expansion: Line out, speaker out, earpiece out, and Power.
	1x GPIO Expansion Header	1x Header for GPIO expansion: 2x10 pin 0.1in	GPIO, SPI, UART, MI²S, and Power.
	1x Sensor Expansion Header	1x Header for sensor expansion: 2x12pin, 0.1in	Accelerometer, Gyro, Magnetometer, Touchscreen, I²C, SPI, and Power.
	1x Debug UART	USB microB	FT232RQ Serial to USB bridge
Connector	3 x board to board connector	Connectors to interface with carrier board	Hirose DF40C series 100pin connector

3.10.4 SOM RF Antenna Interfaces for WIFI/BT and GPS

The SOM includes the following two antenna interfaces:

- WiFi/BT: U.FL type coaxial connector for WCN3680B Wi-Fi/BT Combo Chip
- GPS: U.FL type coaxial connector for WGR7640 GPS RF Front end

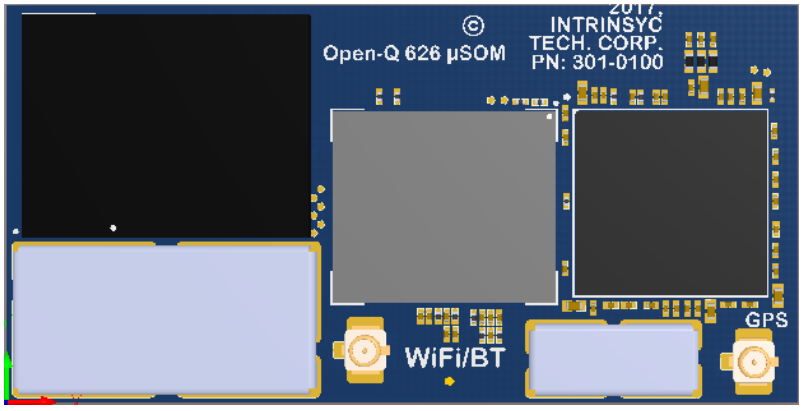


Figure 5 SOM RF Antenna Connectors

Wi-Fi/BT Antenna: By default, the Wi-Fi/BT antenna connector on the SOM is connected to a PCB trace antenna on the carrier board via a coaxial cable and U.FL connector. See section 3.8.12 for more information on the carrier board antenna.

If desired, an external Wi-Fi/BT antenna can be used by removing the coaxial cable and connecting the antenna directly to the U.FL connector on the SOM. Ensure to use only a dual-band 2.4GHz/5GHz antenna meant for the Wi-Fi and Bluetooth bands.

GPS Antenna: By default, the GPS antenna connector on the SOM is connected to a GPS front-end circuit and antenna on the carrier board via a coaxial cable and U.FL connector. The GPS front-end circuit and antenna options on the carrier board are described in more detail in section 3.8.13.

If desired, an external active or passive GPS antenna can be connected directly to the SOM GPS antenna connector. The GPS antenna interface provides 2.7V DC power on the U.FL connector for powering an active antenna. When choosing an antenna make sure that it covers the full frequency range for both GPS and GLONASS as listed below:

GPS: 1574.42 MHz – 1576.42 MHz

GLONASS: 1598 MHz to 1606 MHz

3.11 Open-Q 626 Carrier Board

The Open-Q 626 Carrier board is a Mini-ITX form factor board with various connectors used for connecting to different peripherals. The following are the mechanical properties of the carrier board:

Dimensions	170mm x 170mm (289 cm^2)
Form Factor	Mini-ITX
Major Interfaces	See sections below for details regarding carrier board interfaces

3.11.1 Dip switch S10 Configuration Options

There is a DIP switch S10 on the top side of the Open-Q 626 carrier board. The 8-bit switch allows the user to control the system configuration and boot options. Table 3.8-1 below outlines the pin outs and connections of this DIP switches.

Table 3.2 Dip Switch HW / SW configuration

Function	DIP Switch	Description	Notes
GPS ANT SEL	S10-1	Option to select which antenna to use for GPS. When DIP switch is ON external GPS antenna is connected (SMA connector). When OFF, PCB trace antenna is connected (on-board)	Default out of the box configuration is OFF
FORCED_USB_BOOT	S10-2	Enables FORCE USB (GPIO 37) when DIP switch turned on	Default out of the box configuration is OFF.
BOOT_CONFIG_3	S10-3	Enables APQ boot configuration 3 when DIP switch turned on. Controlled by APQ GPIO109 See schematic for boot configuration options.	Default out of the box configuration is OFF
BOOT_CONFIG_2	S10-4	Enables APQ boot configuration 2 when DIP switch turned on. Controlled by APQ-GPIO107	Default out of the box configuration is OFF
BOOT_CONFIG_1	S10-5	Enables APQ boot configuration 1 when DIP switch turned on. Controlled by APQ-GPIO 113	Default out of the box configuration is OFF

BOOT_CONFIG_0	S10-6	Enables WATCHDOG_DISABLE when DIP switch turned on. Controlled by APQ-GPIO 106	Default out of the box configuration is OFF
CBL_PWR_N	S10-7	Enables the SOM to automatically turn on when input power is applied if this signal is connected to gnd.	Default out of the box configuration is OFF
N/A	S10-8	N/A	N/A

Warning! Before making any changes to the dip switch, make sure to note down the previous configuration. The default switch settings are above.

3.11.2 Battery Power Configuration Switch Options

The carrier board has two switches to control the power source options for the SOM and carrier board:

- Switch S300 – power source select switch – this switch should be set to the “BUCK” position (default) for normal operation from the 12V power input and set to “BATT” position for operation from a battery plugged into the battery connector (J300)
- DIP switch S1 – battery configuration switch:
    - switch S1.3 controls the connection of the battery thermistor to the charging chip. This should be set to ON (default) when no battery is used and should be set to OFF when a battery with a thermistor is connected.
    - Switch S1.4 controls the connection of the battery ID pin to the charging chip. This should be set to ON (default) unless you connect a battery with a valid battery ID pin connected.

See section 3.11.5 for more information about the battery connector and recommended battery.

3.11.3 Carrier Board Expansion Connectors

The following table lists the expansion connectors and their uses on the carrier board:

Table 3.3 Carrier Board Expansion Options and Usage

Domain	Description	Specification	Usage
Power	AC / Barrel charger	12 V DC Power Supply 5 A	Power Supply
	Power connector	20 pin header	For providing extra current to camera connectors when needed (ie: when high

Domain	Description	Specification	Usage
			performance cameras used)
	Battery Connector	6 pin header	For Battery operation and charging development
Debug Serial via USB	Debug Serial UART console over USB for development	Right Angle USB Micro B connector	Development Serial Connector for debug output via USB
Buttons	General Purpose SW button	SMD Button	Additional button for general purpose (connected to APQ_GPIO86)
	Power Button	SMD Button	Power Button for Suspend / Resume and Power off
Zoom / Volume Keys	Volume + key	SMD Button	Volume +Key
	Volume – key	SMD Button	Volume –/Reset Key
Sensor IO Connector	24 pin Sensor Expansion Connectors	Support any user sensor card, Standard 24-pin ST Micro PLCC support via optional daughter card	Available via Lantronix optional accessories kit
GPIO / Education connector Header	20-pin general purpose IO for SPI / I2C / GPIOs/ UIM/ UART functions and other unused GPIOs from PMIC and APQ education header.	Full BLSP1 (SPI/ UART/ I2C/ GPIO) APQ GPIOs MPPs Power	Useful when user wants to use UART GPIOs pins as BLSP other functions (GPIO/ I2C/ UIM/ SPI).
Micro SD (on bottom)	Micro SD card	4bit Micro SD card support	External Storage
Audio Headset Jack	Audio Jack supported using internal CODEC of PM8953	Audio jack providing stereo class-AB headphone amplified output, and mono microphone input.	Audio support

Domain	Description	Specification	Usage
1-Digital Microphone via audio input expansion header	Audio expansion Supported using internal CODEC of PM8953	Digital Audio header	For Digital audio input from DMIC
2-Analog Microphone via audio input expansion header	Audio expansion Supported using internal CODEC of PM8953	Analog Audio header	For Analog audio input from Analog MIC (balanced signal). Provides mic bias.
1-Loud Speaker via audio output expansion header	Audio expansion Supported using internal CODEC of PM8953	Analog Audio header	For loud speaker output after signal has been processed
1-Earpiece via audio output expansion header	Audio expansion Supported using internal CODEC of PM8953	Analog Audio header	For earpiece output after signal has been processed
1-Lineout via audio output expansion header	Audio expansion Supported using internal CODEC of PM8953	Analog Audio header	For balanced lineout output after signal has been processed
HDMI Port	Extended Display ports	HDMI port supports up to 1080P @ 60Hz with embedded HDCP keys to support HDCP 1.3 protocol	External Display
USB 2.0	USB 2.0 via shared USB Type C	USB Type C connector	ADB and USB client / host mode
USB 3.0	USB 3.0 via shared USB Type C	USB Type C connector	Host mode transfer data to and from CPU
WLAN Antenna	1X PCB Antenna	2.4 – 5.1 GHz	Antenna to SOM WiFi module

Domain	Description	Specification	Usage
GPS Antenna	PCB Antenna	GPS: 1574.42 MHz – 1576.42 MHz GLONASS: 1587 MHz – 1606 MHz	Antenna to SOM GPS module
GPS External Antenna via SMA Connector	SMA connector for external GPS antenna	Supports active antenna	External GPS antenna
Coin Cell Holder (Optional)	Coin Cell battery (Optional via stuffing)	Coin cell battery for PMIC RTC	RTC
LED	3xLED	Red: PMIC Driven Green: PMIC Driven Blue: PMIC Driven	Blue: General Purpose MPP_4 Red: Charging Green: Charging complete; General Purpose MPP_2
LCD Display and Touch connector	100 pin for LCD signals via b2b connector to display adapter board	4-lane MIPI DSI0, I2C/SPI/GPIO Backlight MIPI Alliance Specification v1.01 MIPI D-PHY Specification v0.65, v0.81, v0.90, v1.01	Can work as one dual DSI or both independent display
CSI Camera connectors	3 x CSI port connector with CLK, GPIOS, CCI	Supports 3 x Camera interfaces via three separate connectors • 3 x MIPI-CSI each 4 lane • External flash driver control • Support for 3D camera configuration	

Domain	Description	Specification	Usage
		• Separate I2C / CCI control MIPI Alliance Specification v1.00 for Camera Serial Interface	
Power Probe Header	3 pin power probe header	Sense lines connected across 0.005 Ohm resistor	To measure current consumption of SOM
Haptics Connector	2 pin haptics driver header	Haptics driver output from PMI8952	For connecting a 2-pin vibrating motor

The sections below will provide in depth information on each expansion header and connector on the carrier board. The information listed below is of particular use for those who want to interface other external hardware devices with the Open-Q 626. Before connecting anything to the development kit, please ensure the device meets the specific hardware requirements of the interface.

3.11.4 DC Power Input J21

The Open-Q 626 development kit power source connects to the 12V DC power supply jack J21. Starting from the power jack, the 12V power supply branches off into different voltage rails via step down converters on the carrier board and the PMIC on the SOM. The SOM is powered by 3.8V via a Texas Instruments step down converter U400 on the carrier board. To monitor the power going to the SOM, the user can measure the current going into the SOM only via the power probe header J86 (see section below).

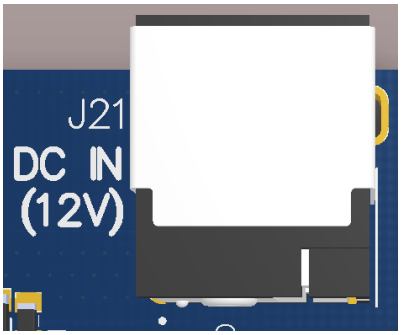


Figure 6 12V DC Power Jack (J21)

3.11.5 Battery Header J300

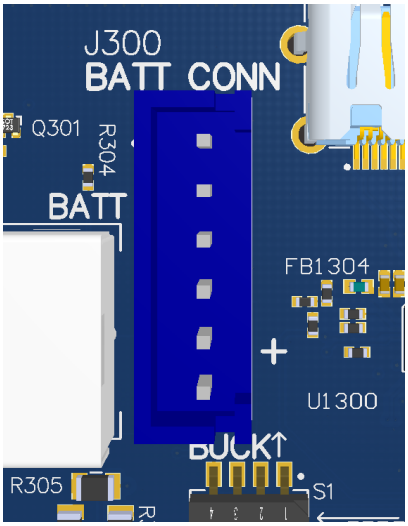


Figure 7 Battery Header (J300)

The Open-Q SOM 626 development platform can also power the SOM with a single cell Lithium-Ion Polymer (LiPo) battery pack which connects to header J300. The purpose of this header is to develop a battery charging solution, including battery characterization. Lantronix recommends using the AA Portable Power Corp's CU-J479-V2 / 1ICP7/55/85 Lithium ion battery pack. This is a single cell pack with a nominal voltage of 3.8V and a capacity of 3200mAh (11.8 Wh, 5A rate). Please note that this battery pack's connector needs to be replaced with the XHP-6 connector housing and SXH-001T-P0.6 contact manufactured by JST Sales America Inc in order to mate correctly with the development kit. The connector pin out of this header is shown below.

Table 3.4 Battery Header Pin Descriptions

Description	Signal	Pin	Note
SOM Battery positive supply terminal	VBAT Plus (VBAT+)	J300[6]	
SOM Battery positive supply terminal	VBAT Plus (VBAT+)	J300[5]	
No Connection	BATT_ID	J300[4]	The recommended battery has no ID connection, therefore keep DIP switch S1.4 in the ON position (see section 3.11.2)
Internal battery pack temperature	BATT_THERM	J300[3]	The recommended battery has a 10K ohm thermistor
SOM Battery negative supply terminal	VBAT Minus(VBAT-)	J300[2]	
SOM Battery negative supply terminal	VBAT Minus(VBAT-)	J300[1]	

Please note that the battery only powers the SOM. To ensure proper functionality of the development kit, the 12V power adapter must still be attached at J21. When a battery is not in use, the TI step down converter U400 is used to power the SOM.

For more information on how to operate the development kit from battery power refer to section 3.11.2.

3.11.6 Power Probe Header J86

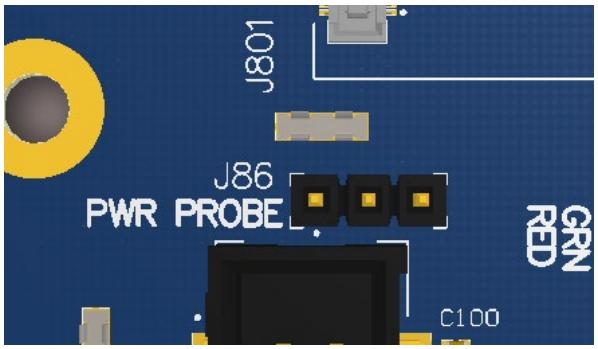


Figure 8 Power Probe Header (J86)

The power probe header is used to sense/ monitor the current on the 3.8V power rail going into the SOM. The table below summarizes the pin outs of header J86.

Table 3.5 SOM Power Probe Header

Description	Signal	Pin
SOM power positive current sense line	SOM_PWR_SENSE_P	J86[1]
SOM power negative current sense line	SOM_PWR_SENSE_N	J86[2]
GND	GND	J86[3]

3.11.7 Debug Serial UART over USB J22

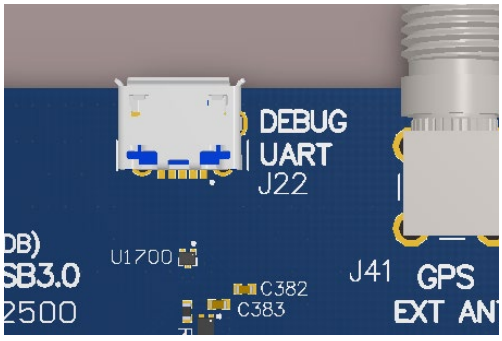


Figure 9 Debug UART over USB (J22)

The UART connection used on the Open-Q 626 is a USB micro B connector (J22). This debug UART is available over USB via the FTDI FT232RQ chip on the carrier board. To get the serial terminal working with a PC, user needs to ensure that the appropriate FTDI drivers are installed.

3.11.8 Sensor IO Expansion Header J53

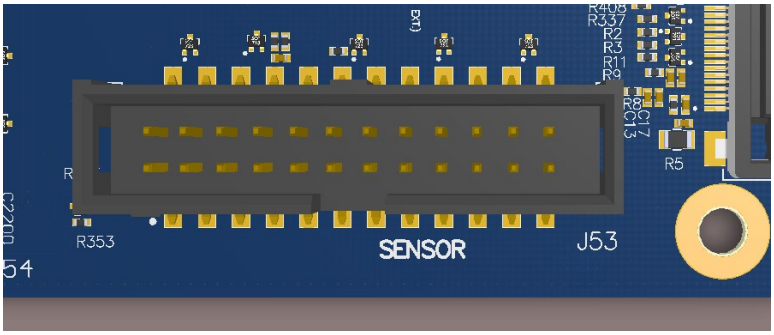


Figure 10 Sensor Expansion Header (J23)

The sensor expansion header J53 allows for a 24-pin connection to an optional sensor board. If user application does not require a sensor, then this header can be used for other applications that require I2C or GPIO input and output connections.

Following is the pin breakout for sensor expansion header J53.

Table 3.6 Sensor Expansion Header J53 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
I²C serial data	GPIO_6_BLSP2_I2C_SDA	J53[1]	Accelerometer interrupt input to processor via GPIO117	GPIO_42_ACCEL_INT	J53[2]
I²C serial clock	GPIO_7_BLSP2_I2C_SCL	J53[3]	Cap interrupt input to processor via GPIO13	GPIO_13_CAP_INT_N	J53[4]
Sensor reset signal from processor to sensor via GPIO127	GPIO_127	J53[5]	Gyroscope interrupt input to processor via GPIO45	GPIO_45_GYRO_INT	J53[6]

Description	Signal	Pin NO	Description	Signal	Pin NO
Sensor IO PWR 1.8V VREG_L6_1P8 power supply regulator (Digital)	VREG_L6_1P8	J53[7]	Sensor Analog power supply from VREG_L10_3P0 or 3.3V (If R160 populated)	SENS_ANA_PWR	J53[8]
GND	GND	J53[9]	GND	GND	J53[10]
HRM interrupt/ configurable GPIO140	GPIO_140_HRM_INT	J53[11]	Touch screen interrupt input from processor via GPIO65	GPIO_65_TS_INT_N	J53[12]
SPI chip select1	GPIO_48_SPI6_CS1_MAG_N	J53[13]	Alternate sensor interrupt input to processor via GPIO43	GPIO_43_ALSP_INT_N	J53[14]
NC	NC	J53[15]	Digital Compass interrupt input to processor via GPIO44	GPIO_44_MAG_DRDY_INT	J53[16]
NC	NC	J53[17]	NC	NC	J53[18]
SPI chip select0	GPIO_22_SPI6_CS_N	J53[19]	SPI data master out/ slave in	GPIO_20_SPI6_MOSI	J53[20]
SPI clock	GPIO_23_SPI6_CLK	J53[21]	SPI data master in/ slave out	GPIO_21_SPI6_MISO	J53[22]
NC	NC	J53[23]	Power enable via GPIO35	GPIO_35_CCI_TIMER2	J53[24]

3.11.9 MISC GPIO header J54

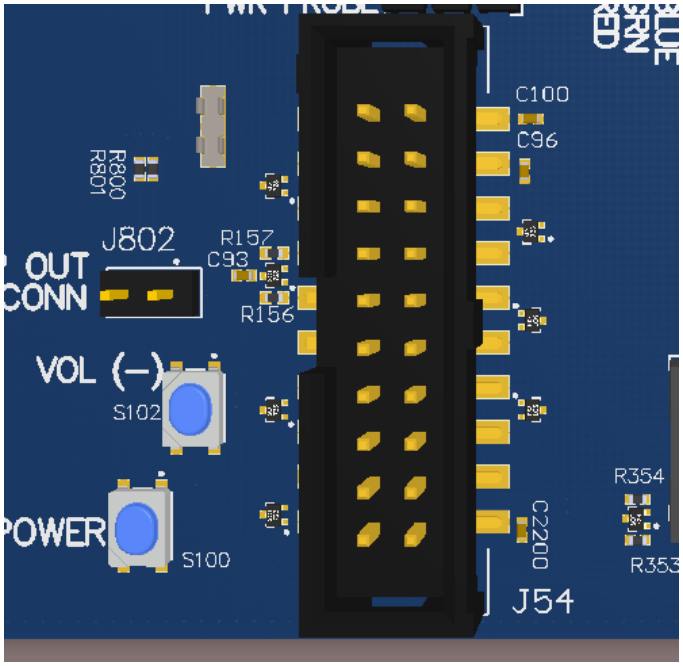


Figure 11 MISC GPIO header (J54)

MISC GPIO header J54 is a 20 pin connector that provides access to BLSP1, UART, MI²S, and GPIO signals. It is ideally used for connecting external peripherals such as microcontrollers and any other devices that are based on I2C, SPI, UART, I²S, and GPIO. Please refer to the SOM carrier board schematic for target voltage and current rating depending on stuffing option. The header also supports multiple voltage ratings.

The table below outlines the power available on the header:

Table 3.7 GPIO Header Power Outputs

Voltage Rails	Current available
MB_VREG_3P3 – 3.3 V	300 mA
VREG_L5_1P8 – 1.8V	150 mA
MB_VREG_5P0 – 5.0 V	150 mA

The following are the detailed pin out information for education header J54.

Table 3.8 MISC GPIO Header J54 Pin Out

Description	Signal	Pin NO	Description	Signal	Pin NO
NC	NC	J54[1]	VREG_L5 1.8V voltage regulator max 150mA	VREG_L5_1P8	J54[2]
BLSP1 SPI MOSI	GPIO_0_BLSP1_SPI_MOSI	J54[3]	3.3V Power Supply max 300mA	MB_VREG_3P3	J54[4]
BLSP1 SPI MISO	GPIO_1_BLSP1_SPI_MISO	J54[5]	MI2S MCLK	GPIO_66_SEC_MI2S_MCLK_B	J54[6]
BLSP1 SPI CS	GPIO_2_BLSP1_SPI_SPI_CS_N	J54[7]	PM8953 MPP3	PM_MPP_3	J54[8]
BLSP1 SPI CLK	GPIO_3_BLSP1_SPI_CLK	J54[9]	MI2S D3	GPIO_95_MI2S_1_D3	J54[10]
NC	NC	J54[11]	MI2S D0	GPIO_93_MI2S_1_D0	J54[12]
UART TX	GPIO_16_BLSP5_UART_TX	J54[13]	MI2S D1	GPIO_88_MI2S_1_D1	J54[14]
UART RX	GPIO_17_BLSP5_UART_RX	J54[15]	MI2S WS	GPIO_92_MI2S_1_WS	J54[16]
GND	GND	J54[17]	MI2S D2	GPIO_94_MI2S_1_D2	J54[18]
MI2S SCK	GPIO_91_MI2S_1_SCK	J54[19]	5V power supply max 150mA	MB_VREG_5P0	J54[20]

3.11.10 Audio Headset Jack J27

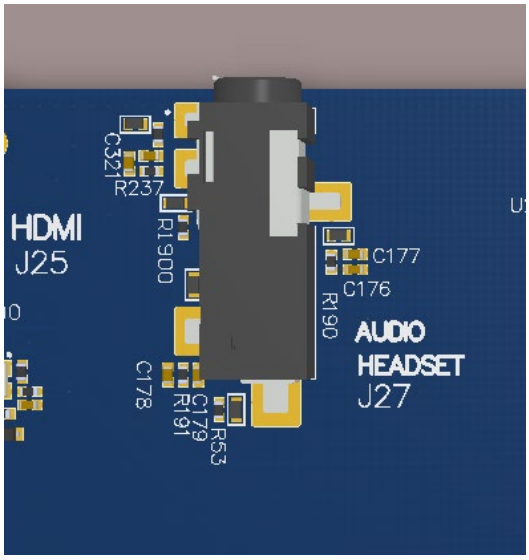


Figure 12 Audio Headset Jack (J27)

The Audio headset jack (J27) is a 3.5mm TRRS jack. It is compatible with standard headset jacks.

3.11.11 Audio Input Expansion Header J50

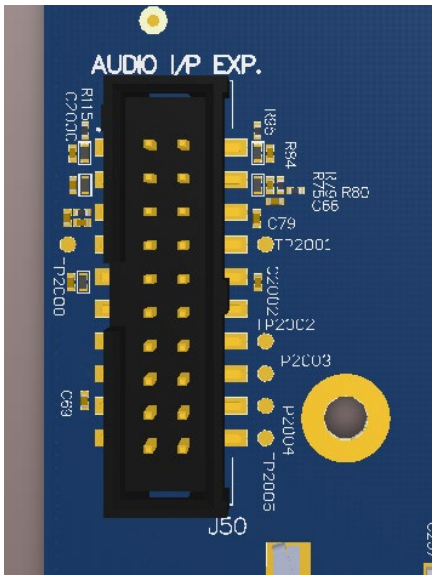


Figure 13 Audio Input Expansion Header (J50)

This header expansion provides the following audio inputs:

1. 1 digital mic input (can support 2 digital microphones)
2. 2 analog mics
3. Voltage rails to support analog and digital mics

For details on how to connect analog or digital microphones to system, see document R-2.

The table below outlines the pin out information of the audio input expansion header J50:

Table 3.9 Audio Input Expansion Header J50 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog MIC1 positive balanced input	CDC_MIC1_P	J50[1]	Analog MIC1 negative balanced input	CDC_MIC1_N	J50[2]
Analog MIC3 positive balanced input	CDC_MIC3_P	J50[3]	Analog MIC3 negative balanced input	CDC_MIC3_N	J50[4]
MIC bias output voltage 1	CDC_MIC_BIAS 1	J50[5]	MIC bias output voltage 1	CDC_MIC_BIAS1	J50[6]
Test Point	TP2000	J50[7]	Test Point	TP2001	J50[8]
MIC bias output voltage 1	CDC_MIC_BIAS 1	J50[9]	3.3V power supply max 500mA	MB_VREG_3P3	J50[10]
GND	GND	J50[11]	GND	GND	J50[12]
Clock for digital MIC	GPIO_89_DMIC 0_CLK	J50[13]	Connected to Test Point	TP2002	J50[14]
Data for digital MIC	GPIO_90_DMIC 0_DATA	J50[15]	Connected to Test Point	TP2003	J50[16]
1.8V power supply max 300mA	VREG_L5_1P8	J50[17]	Connected to Test Point	TP2004	J50[18]
GND	GND	J50[19]	Connected to Test Point	TP2005	J50[20]

3.11.12 Audio Output Expansion Header J26

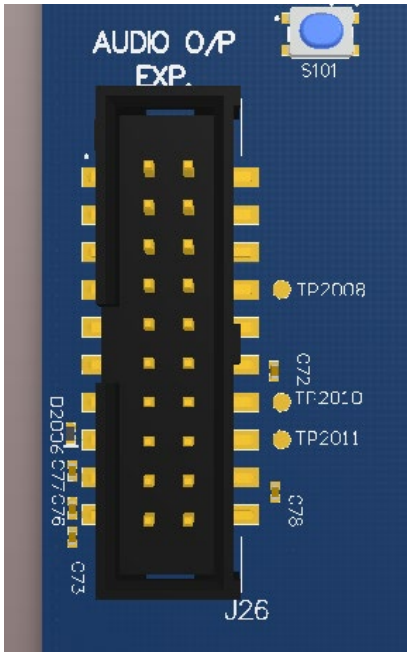


Figure 14 Audio Output Expansion Header (J26)

This header expansion provides the following audio outputs:

1. 1 balanced analog audio line out
2. 1 balanced analog audio amplified output (no external amp needed)
3. 1 balanced analog earpiece output
4. 1 GPIO from the PMI8952
5. Voltage rails to support analog and digital mics

The table below outlines the pin out information of the audio outputs expansion header J26:

Table 3.10 Audio Output Expansion Header J26 Pin out

Description	Signal	Pin NO	Description	Signal	Pin NO
Analog audio line out, positive balanced output	CDC_LINEOUT_P	J26[1]	Analog audio line out, negative balanced output	CDC_LINEOUT_N	J26[2]
Analog audio amplified out, positive balanced output	CDC_SPKR_DRV_P	J26[3]	Analog audio amplified out, negative balanced output	CDC_SPKR_DRV_N	J26[4]

Description	Signal	Pin NO	Description	Signal	Pin NO
Connected to Test Point	TP2006	J26[5]	3.3V output power supply	MB_VREG_3P3	J26[6]
Connected to Test Point	TP2007	J26[7]	Connected to Test Point	TP2008	J26[8]
Analog earpiece out, positive balanced output	CDC_EAR_P	J26[9]	Analog earpiece out, negative balanced output	CDC_EAR_N	J26[10]
GND	GND	J26[11]	3.8V output power supply	SOM_SYS_PWR_PER	J26[12]
Connected to Test Point	TP2009	J26[13]	Connected to Test Point	TP2010	J26[14]
GPIO from PMI8952	PMI_GPIO_1	J26[15]	Connected to Test Point	TP2011	J26[16]
1.8V output power supply	VREG_L5_1P8	J26[17]	12V output power supply	DC_IN_12V	J26[18]
5.0V output power supply	MB_VREG_5P0	J26[19]	GND	GND	J26[20]

3.11.13 On-board PCB WLAN Antenna

The Open-Q 626 carrier board has an on-board WLAN PCB antenna that connects to the WCN3680B WiFi module on the SOM. The connection is via a coaxial cable that attaches to U.FL receptacles. The antenna connects to the SOM in the following configuration - WiFi/BT on SOM WCN3680B WiFi module to WLAN1/BT COAX on carrier.

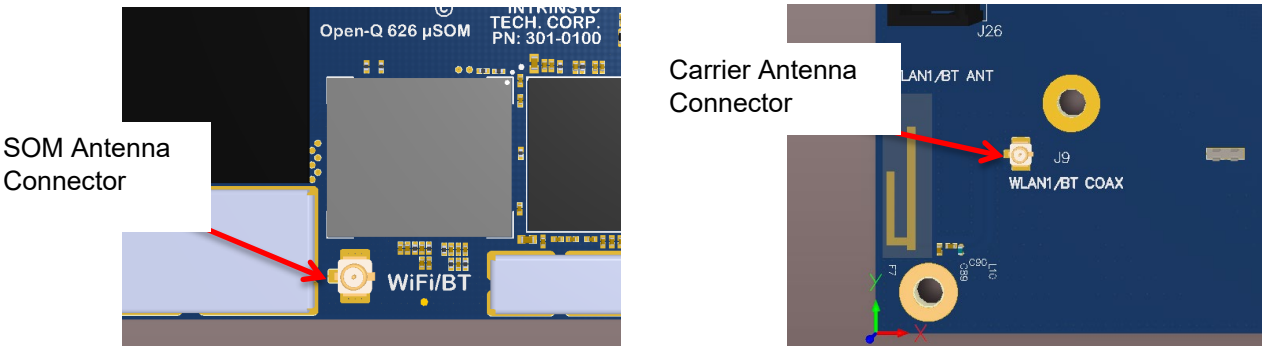


Figure 15 On-board PCB Trace Antenna for Wi-Fi/BT

3.11.14 Carrier Board GPS Front-end and Antenna Options

The Open-Q 626 carrier board provides a GPS front-end circuit and on-board PCB trace antenna for user convenience. The front-end circuit consists of a high-performance GPS low noise amplifier (LNA), a band pass filter (BPF), and an antenna switch. The antenna switch provides the flexibility to connect to the on-board PCB trace antenna or the SMA connector for an external antenna. To select which antenna option to use, set the dip switch, S10, correctly as shown below in Table 3.11.

The power for the LNA on the carrier board is provided from the SOM active antenna power (2.7V DC), via the coaxial cable. This power is also passed through the carrier board front-end circuit to the SMA external antenna connector so it can power an active external antenna. If using an active external antenna ensure that it is meant to operate from 2.7V.

Table 3.11 GPS Antenna Selection Switch

GPS Antenna Selection	Dip Switch S10 (Position 1) Selection
On Board PCB Antenna	Off Position
External antenna (supports active or passive antennas)	On Position

3.11.15 Open-Q Display

The display output options for the Open-Q 626 Development Kit consists of:

- An HDMI type A connector
  - HDMI port supports up to 1080P @ 60Hz
- A 100-pin display connector J2 that supports:
  - MIPI-DSI DPHY 1.2 (up to 1920 x 1200 at 60 fps)
  - Touch screen capacitive panel via I2C or SPI, and interrupts (up to one device)
  - Backlight LED
    - Can support external backlight driver control and power
    - PMI8952 backlight driver supports three LED strings of up to 30mA each with 28V maximum boost voltage

The Open-Q 626 development platform can support the following display combinations:

MIPI DSI	1 x 4-lane DSI 1 x 4-lane DSI DPHY 1.2 and HDMI (1080P60) Display 1920 x 1200 at 60fps, 2560 buffer width (10 layers blending)
HDMI	1080P @ 60 Hz

3.11.16 HDMI Connector J25

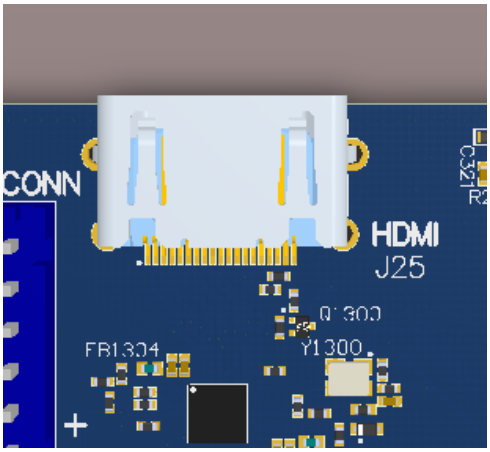


Figure 16 HDMI Type A Connector (J25)

The on-board HDMI type A connector enables the Open-Q 626 development platform to connect to an external HDMI monitor/ television via an HDMI cable. The APQ8053-Pro does not have a native HDMI interface. A MIPI-DSI to HDMI bridge IC (ADV7535) is used to enable an HDMI transmitter which supports video resolutions up to a maximum TMDS clock frequency of 148.5 MHz. With the inclusion of embedded HDCP keys, the ADV7535 allows the secure transmission of protected content, as specified by the HDCP 1.3 protocol.

Please note that the Open-Q 626 Development kit is for evaluation purposes only and may not be HDMI compliant.

3.11.17 Display Connector J2

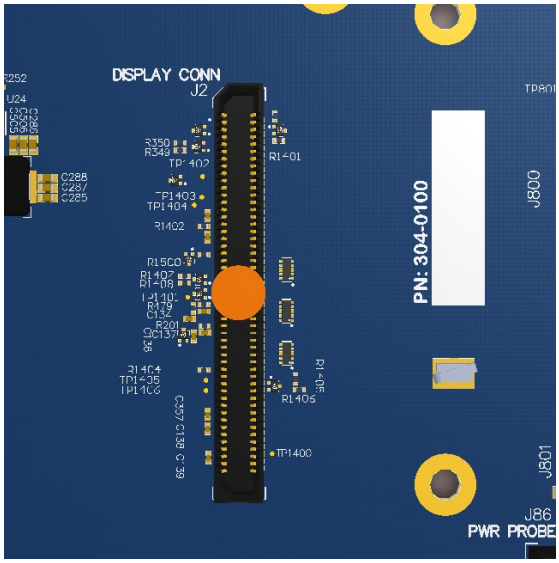


Figure 17 100-Pin Display Connector (J2)

The 100-pin display connector provides the following features and connections that enable the development kit to connect to a MIPI DSI display panel device:

Note: Please refer to the carrier board schematic and display board tech note when designing a custom display board.

- DSI
  - 1 x 4 lane DSI
- Backlight
  - Built-in backlight WLED driver on PMI8952
    - WLED driver supports up to 28V output for backlight
  - Primary external backlight (BL0)
    - Backlight control signals
    - External Power
- Display connector – LCD/ AMOLED
  - PMI8952 programmable display bias output voltage:
    - 5V to 6.1V and -1.4V to -6.0V (LCD display)
    - 4.6V to 5V and -1.4V to -5.4V (AMOLED display)
- Additional GPIOs for general purposes available
- VREG_L6_1P8 voltage rail from PM8953
  - Required by display for DOVDD
  - 300mA current path
- Touch Panel
  - Supports one touch screen controller
  - Supports I2C or SPI via BLSP3

Power specifications:

The display connector supports the following power domains:

Table 3.12 Display Connector Power Outputs

Display Signal	Power Domain
PM8953 LDO10 (1.75V - 3.3375V)	up to 150 mA
PM8953 LDO6 (1.75V- 3.3375V)	up to 300 mA
Carrier 3.3V	up to 0.5A
Carrier 5V	up to 1.5A
Carrier 12V	up to 0.5A

Lantronix offers an optional display adapter board accessory to the Open-Q 626 development kit. This display adapter mates with the display connector J2 on the carrier board and allows users to interface with the development kit via the LCD panel. To purchase this, please visit http://shop.intrinsyc.com or contact Lantronix at sales@lantronix.com for details. The following figure illustrates how the display adapter connects to the development kit.

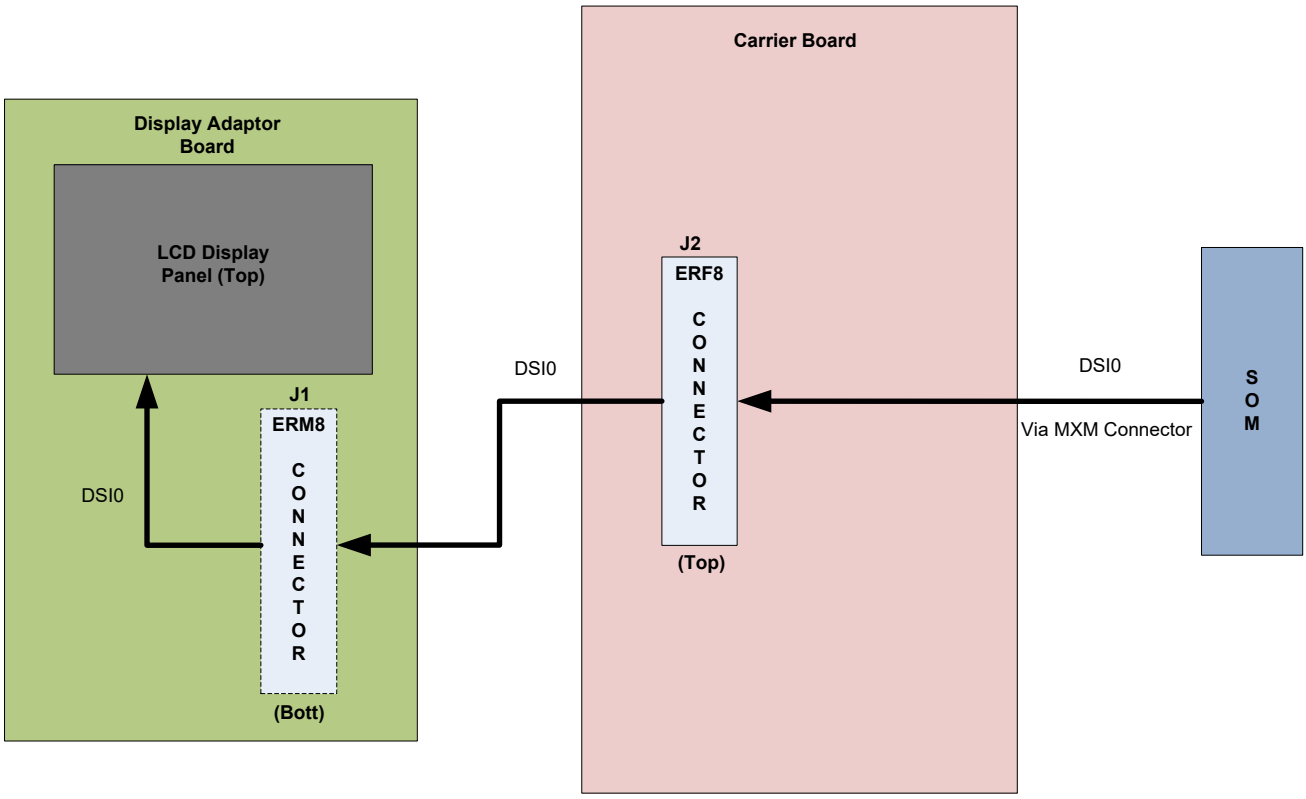


Figure 18 Display Board Default Configuration

Below are the LCD panel specifications of the display adapter:

- **Resolution:** 480x854
- **LCD Type:** IPS
- **PCAP** touch panel with cover glass
- **No of Lanes:** 1 x 2 lane MIPI DSI interface via Display Board.
- **Diagonal Length**: 4.5”

3.11.18 Camera Connectors

The Open-Q 626 development kit supports three 4-lane MIPI CSI camera interfaces via three separate JAE 41-pin connectors.

The following are some features of the camera connectors:

- 3 x 4 lane MIPI CSI signals
- No support for integrated flash driver
- Support for 3D camera configuration
- Separate I2C control (CCI0, CCI1)
- Supports all three CSI interfaces
- All camera CSI connectors are on the carrier board edge
- Self-regulated camera modules can be powered with 3.3V power (MB_VREG_3P3)
- Uses JAE FI-RE41S-VF connector for exposing MIPI, CLK, GPIOs and Power rails.
- Please use JAE FI-RE41S-HF to mate with the camera connectors on the carrier board
- Lantronix offers a 13MP camera module as an optional accessory to the Open-Q 626 development kit. The camera module comes with a ribbon cable connector to mate to the camera connectors on the carrier board. To purchase this accessory, please visit http://shop.intrinsyc.com or contact Lantronix at sales@lantronix.com for details.

Figure 19, below, shows the three MIPI CSI camera connectors on the carrier board.

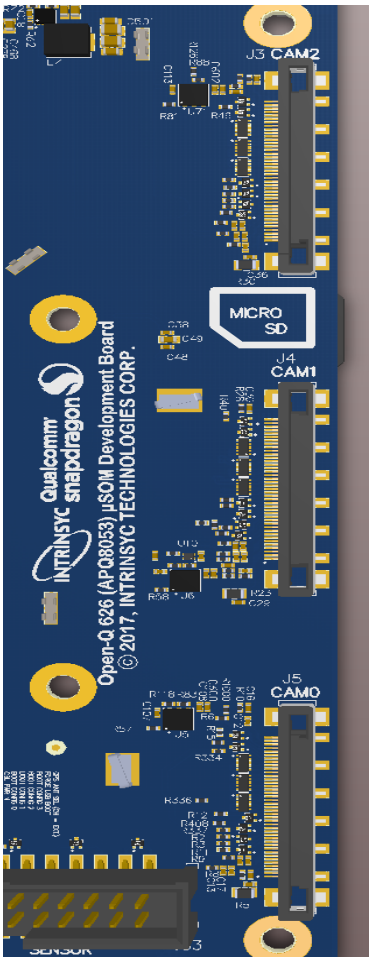


Figure 19 Camera Connectors (J5, J4, J3)

The table below describes the pin-out and details of the camera connectors.

Table 3.13 MIPI CSI Camera Connector Pinouts (J5, J4, J3)

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
1, 2, 3	MB_VREG_3P3	MB_VREG_3P3	MB_VREG_3P3	Power output. Connected to main +3.3V MB_VREG_3P3 max current 700mA
4	GND	GND	GND	Ground
5	VREG_L17_2P85	VREG_L17_2P85	VREG_L17_2P85	Power output. Connected to PM8953 VREG_L17 regulator. Default is +2.85V. Maximum current 300mA
6	MB_ELDO_CAM0_DVDD	MB_ELDO_CAM1_DVDD/VREG_L2_1P1 (DNP)	MB_ELDO_CAM2_DVDD/VREG_L2_1P1 (DNP)	Power output. Connected to U5, U6, and U71 AMS LDO regulator. Default is +1.1V. Maximum current 1A
7, 8	VREG_L22_2P85	MB_ELDO_CAM1_VCM/ VREG_L22_2P85 (DNP)	VREG_L22_2P85	Power output. Connected to PM8953 VREG_L22 regulator. Default is +2.85V. Maximum current 150mA. For CAM1 J4, U10 is used. Default is 2.8V and maximum current is 300mA
9, 10	VREG_L6_1P8	VREG_L6_1P8	VREG_L6_1P8	Power output. Connected to PM8953 VREG_L6 LDO output. Default is +1.8V. Maximum current 300mA
11	GND	GND	GND	Ground
12	CAM0_FLASH_EN (APQ_GPIO33)	CAM1_FLASH_EN (DNP) (APQ_GPIO33) Install R36 to access signal	CAM2_FLASH_EN (DNP) (APQ_GPIO33) Install R42 to access signal	Output. Connected to APQ8053. Default use is for camera flash strobe enable
13	CAM1_RST_N (APQ_GPIO40)	CAM2_RST_N (APQ_GPIO129)	CAM3_RST_N (APQ_GPIO131)	Output. Connected to APQ8053 GPIO40 / GPIO129 / GPIO131.

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
				Default use is for camera reset
14	CAM1_STANDBY_N (APQ_GPIO39)	CAM2_STANDBY_N (APQ_GPIO130)	CAM3_STANDBY_N (APQ_GPIO132)	Output. Connected to APQ8053 GPIO39 / GPIO130 / GPIO132. Default use is for camera standby
15	CCI_I2C_SCL0 (APQ_GPIO30)	CCI_I2C_SCL0 (APQ_GPIO30)	CCI_I2C_SCL0 (APQ_GPIO30)	Output. Connected to APQ8053 GPIO30. Default use is for camera CCI0 I2C clock interface
16	CCI_I2C_SDA0 (APQ_GPIO29)	CCI_I2C_SDA0 (APQ_GPIO29)	CCI_I2C_SDA0 (APQ_GPIO29)	Input / output. Connected to APQ8053 GPIO29. Default use is for camera CCI0 I2C data interface
17	CAM_MCLK0_BUF (APQ_GPIO26)	CAM_MCLK1_BUF (APQ_GPIO27)	CAM_MCLK2_BUF (APQ_GPIO28)	Output. Connected to APQ8053 GPIO26 / GPIO27 / GPIO28. Default use is for camera master clock. Maximum 24MHz
18	FLASH_STROBE_TRIG (APQ_GPIO34)	FLASH_STROBE_TRIG (DNP) (APQ_GPIO34) Install R37 to access signal	FLASH_STROBE_TRIG (DNP) (APQ_GPIO34) Install R43 to access signal	Output. Connected to APQ8053 GPIO34. Default use is for camera flash strobe trigger
19	GND	GND	GND	Ground
20	MIPI_CSI0_LANE0_N	MIPI_CSI1_LANE0_N	MIPI_CSI2_LANE0_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
21	MIPI_CSI0_LANE0_P	MIPI_CSI1_LANE0_P	MIPI_CSI2_LANE0_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 0
22	GND	GND	GND	Ground
23	MIPI_CSI0_CLK_N	MIPI_CSI1_CLK_N	MIPI_CSI2_CLK_N	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
24	MIPI_CSI0_CLK_P	MIPI_CSI1_CLK_P	MIPI_CSI2_CLK_P	Input. MIPI CSI0 / CSI1 / CSI2 clock lane
25	GND	GND	GND	Ground

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
26	MIPI_CSI0_LANE1_N	MIPI_CSI1_LANE1_N	MIPI_CSI2_LANE1_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
27	MIPI_CSI0_LANE1_P	MIPI_CSI1_LANE1_P	MIPI_CSI2_LANE1_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 1
28	GND	GND	GND	Ground
29	MIPI_CSI0_LANE2_N	MIPI_CSI1_LANE2_N	MIPI_CSI2_LANE2_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
30	MIPI_CSI0_LANE2_P	MIPI_CSI1_LANE2_P	MIPI_CSI2_LANE2_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 2
31	GND	GND	GND	Ground
32	MIPI_CSI0_LANE3_P	MIPI_CSI1_LANE3_P	MIPI_CSI2_LANE3_P	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
33	MIPI_CSI0_LANE3_N	MIPI_CSI1_LANE3_N	MIPI_CSI2_LANE3_N	Input. MIPI CSI0 / CSI1 / CSI2 data lane 3
34	GND	GND	GND	Ground
35	CCI_I2C_SDA1 (APQ_GPIO31)	CCI_I2C_SDA1 (APQ_GPIO31)	CCI_I2C_SDA1 (APQ_GPIO31)	Output / Input. Connected to APQ8053 GPIO31. Default use is for camera CCI1 I2C data interface
36	CCI_I2C_SCL1 (APQ_GPIO32)	CCI_I2C_SCL1 (APQ_GPIO32)	CCI_I2C_SCL1 (APQ_GPIO32)	Output. Connected to APQ8053 GPIO32. Default use is for camera CCI1 I2C clock interface
37	CAM0_IRQ (APQ_GPIO12)	CAM1_IRQ (DNP) (APQ_GPIO12) Install R40 to access signal	CAM_IRQ (DNP) (APQ_GPIO12) Install R46 to access signal	Input. Connected to APQ8053 GPIO12. CAM_IRQ signal
38	CAM0_MCLK3 (APQ_GPIO128)	CAM1_MCLK3 (DNP) (APQ_GPIO128) Install R41 to access signal	CAM2_MCLK3 (DNP) (APQ_GPIO128) Install R47 to access signal	Output. Connected to APQ8053 GPIO128. Default NC. Use is for secondary camera master clock. Maximum 24MHz

Pin#	CAM0 (J5)	CAM1 (J4)	CAM2 (J3)	Description
39	MB_ELDO_CAM0_DVDD	MB_ELDO_CAM1_DVDD/VREG_L2_1P1 (DNP)	MB_ELDO_CAM2_DVDD/VREG_L2_1P1 (DNP)	Power output. Connected to U5, U6, and U71 AMS LDO regulator. Default is +1.1V. Maximum current 1A
40, 41	MB_VREG_5P0 (DNP) Install R10 to access rail	MB_VREG_5P0 Install R28 to access rail	MB_VREG_5P0 Install R35 to access rail	Power output. 5V Power supply. Maximum 700mA

Note: A connection from the camera connectors on the carrier board to the In Lantronix camera adapter board is established by a 41-pin cable assembly from JAE Electronics (part number JF08R0R041020MA). This cable assembly is included with the purchase of the Lantronix 13MP camera accessory.

The following table shows the combinations of camera usage for different use cases.

Table 3.14. MIPI CSI Camera Use Cases

CSI PHY	Use case	Comment
CSI0	Up to 4 lanes	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 1	Up to 4 lanes	One Camera of 4 lane or One camera of 3 lane One Camera of 2 lane One Camera of 1 lane
CSI 2	Up to 4 lanes	One Camera of 4 lane or 2 x Camera of 1 lane each
CSI0 + CSI1	Up to 4 lane 3D	4 lane 3D use case / Dual 4 lane configuration
CSI 2	Up to 1 lane 3D	1 lane 3D use case / Dual 1 lane configuration
CSI0 + CSI1 + CSI2	Up to 4 lanes	Three 4-lane CSI (4+4+4 or 4+4+2+1)
CPHY		Three 3-trio CPHY1.0

3.11.19 Power Header via 20 Pin Connector J60

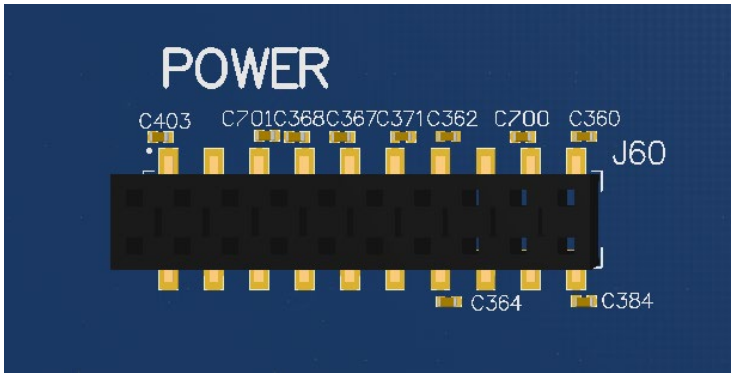


Figure 20 Power Connector (J60)

The power header, J60, provides the following:

- For providing camera connectors with additional current than what is originally supported by on board regulators. This is to mitigate the effect of high resistance and IR drop on flat cables which can violate camera sensor requirements for high performance cameras
- It is recommended to use this when high performance (high mega pixels) cameras are being used. Usually high-performance cameras require more power
- Can also be used as a general power header if user would like to use voltage rails brought out to this connector.

See the table below for details of the power header pin-out.

Table 3.15 Power Header Pin-out

Description	Signal	Pin NO	Description	Signal	Pin NO
1.1V power rail for camera 0	MB_ELDO_CAM0_DVDD	J60[1]	2.85V power rail for camera 0 (AVDD)	VREG_L17_2P85	J60[2]
NC	NC	J60[3]	GND	GND	J60[4]
1.8V power rail for camera 0, 1, 2	VREG_L4_1P8	J60[5]	3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[6]
1.1V power rail for camera 1	MB_ELDO_CAM1_DVDD	J60[7]	2.85V power rail for camera 1 (AVDD)	VREG_L17_2P85	J60[8]

Description	Signal	Pin NO	Description	Signal	Pin NO
2.8V power rail for camera 1 (VDD)	MB_ELDO_CAM1_VCM	J60[9]	GND	GND	J60[10]
1.8V power rails for camera 0, 1, 2	VREG_L4_1P8	J60[11]	3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[12]
1.1V power rail for camera 2	MB_ELDO_CAM2_DVDD	J53[13]	2.85V power rail for camera 2 (AVDD)	VREG_L22_2P85	J60[14]
NC	NC	J53[15]	GND	GND	J60[16]
1.8V power rail for camera 0, 1, 2	VREG_L4_1P8	J60[17]	3.3V power rail for camera 0, 1, 2	MB_VREG_3P3	J60[18]
5V power rail for camera 0, 1, 2	MB_VREG_5P0	J60[19]	12V power rail for camera 0, 1, 2	DC_IN_12V	J60[20]

3.11.20 USB 2.0 Client Port Operation

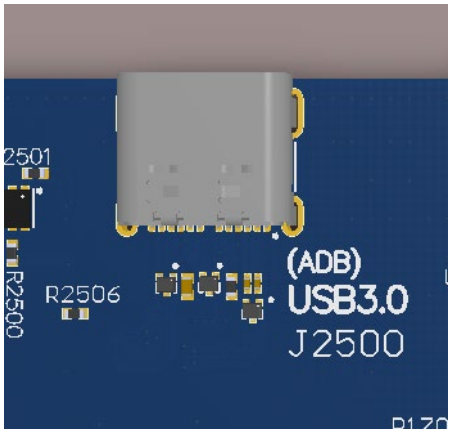


Figure 21 USB2.0 for ADB (J2500)

J2500 allows the development kit to communicate with a host PC using the Android Debug Bridge (ADB). This port uses a USB Type C connector, which contains both USB 2.0 (client mode port only) and USB3.0

SuperSpeed ports. To use the USB 2.0 port, connect a USB 3.0 Type C to Standard Type A data cable, or equivalent adapter, to J2500.

Figure 22 USB Type C to USB 2.0 Cable

3.11.21 USB 3.0 Interface Operation

J2500 allows the development kit to communicate as a SuperSpeed host, when a USB 3.0 device is connected via a direct connection (e.g. USB Type C memory stick), USB Type C to Type C cable, or USB Type C to USB 3.0 cable, is used.

Figure 23 Example USB Type C Memory Stick

Figure 24 USB Type C to Type C Cable

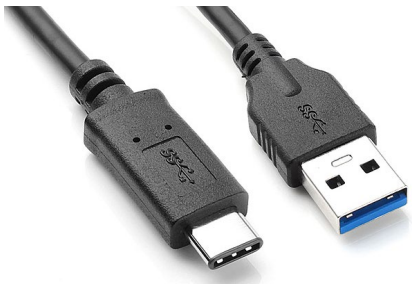


Figure 25 USB Type C to USB 3.0 Type A Cable