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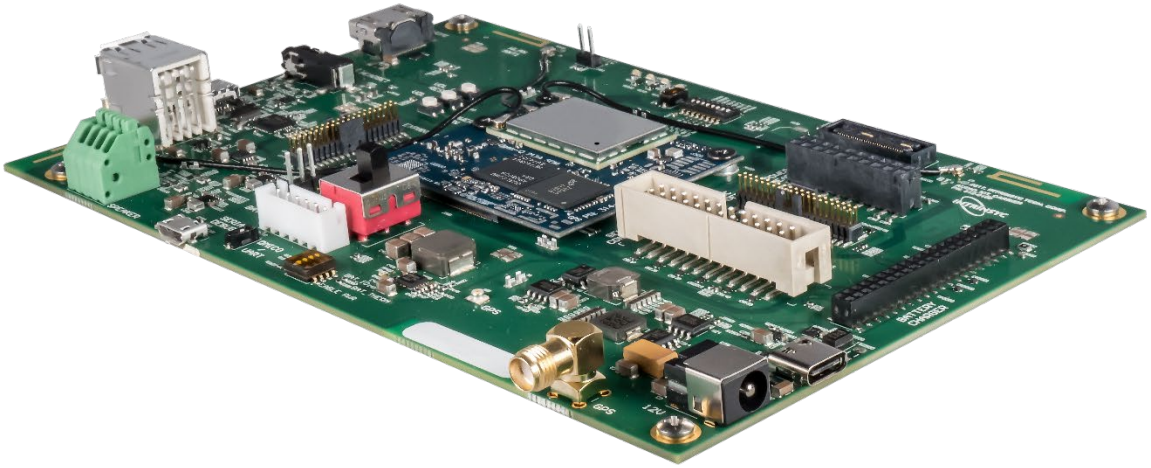

Open-Q™ 212A Development Kit User Guide

Part Number PMD-00077

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Revision History

Date	Rev.	Comments
May 2019	1.0	Initial release. Intrinsyc document number: ITC-01RND1324-UG-001
August 2020	A	Initial Lantronix document. Added Lantronix document part number, Lantronix logo, branding, contact information, and links.

For the latest revision of this product document, please go to: http://tech.intrinsyc.com.

Contents

1 Introduction

1.1 Purpose

The purpose of this user guide is to provide primary technical information on the Open-Q™ 212A Development Kit which is based on the Qualcomm® Snapgradon 212 (APQ8009) processor.

For more background information on this development kit, visit: https://www.lantronix.com/products/open-q-212a-home-hub-development-kit/

1.2 Scope

This document will cover the following items on the Open-Q 212A:

- Block Diagram and Overview
- Hardware Features
- Configuration
- SOM
- Carrier Board
- Accessories

1.3 Intended Audience

This document is intended for users who would like to develop custom applications on the Lantronix Open-Q 212A Development Kit.

2 Documents

This section lists the supplementary documents for the Open-Q 212A development kit.

2.1 Applicable Documents

Reference	Title
A-1	Intrinsyc Purchase and Software License Agreement for the Open-Q Development Kit

2.2 Reference Documents

Reference	Title
R-1	
R-2	Open-Q™ 212A Schematics (SOM, Carrier)

2.3 Terms and Acronyms

Term and acronyms	Definition
AMIC	Analog Microphone
ANC	Audio Noise Cancellation
B2B	Board to Board
BLSP	Bus access manager Low Speed Peripheral (Serial interfaces like UART / SPI / I2C/ UIM)
BT LE	Bluetooth Low Energy
CSI	Camera Serial Interface
DSI	MIPI Display Serial Interface
EEPROM	Electrically Erasable Programmable Read only memory
eMMC	Embedded Multimedia Card
FCC	US Federal Communications Commission
FWVGA	Full Wide Video Graphics Array

Term and acronyms	Definition
GPS	Global Positioning system
GNSS	Global Navigation Satellite System
HDMI	High Definition Media Interface
HSIC	High Speed Inter-Connect Bus
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MIPI	Mobile Industry processor interface
MPP	Multi-Purpose Pin
NFC	Near Field Communication
RF	Radio Frequency
SATA	Serial ATA
SLIMBUS	Serial Low-power Inter-chip Media Bus
SOM	System On Module
SPMI	System Power Management Interface (Qualcomm PMIC / baseband proprietary protocol)
SSBI	Single wire serial bus interface (Qualcomm proprietary mostly PMIC / Companion chip and baseband processor protocol)
UART	Universal Asynchronous Receiver Transmitter
UFS	Universal Flash Storage
UIM	User Identity module
USB	Universal Serial Bus
USB HS	USB High Speed
USB SS	USB Super Speed

2.4 List of Figures

2.5 List of Tables

3 Open-Q 212A Development Kit

3.1 Introduction

The Open-Q 212A provides a reference and evaluation platform for the Qualcomm 212 processor. This kit is suited for Linux Home Hub OS testing to evaluate, optimize, and deploy applications that utilize the Qualcomm 212 series SOC technology.

3.2 Development Platform Notice

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

This development platform may only be used in a controlled user environment where operators have obtained the necessary regulatory approvals for experimentation using a radio device and have appropriate technical training. The device may not be used by members of the general population or other individuals that have not been instructed on methods for conducting controlled experiments and taking necessary precautions for preventing harmful interference and minimizing RF exposure risks. Additional RF exposure information can be found on the FCC website at http://www.fcc.gov/oet/rfsafety/

3.3 Anti-Static Handling Procedures

The Open-Q 212A Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist or foot strap

3.4 Kit Contents

The Open-Q 212A Development Kit includes the following:

- Open-Q 212A SOM with the Qualcomm 212 (APQ8009) processor
- Open-Q 212A Carrier board
- AC power adapter

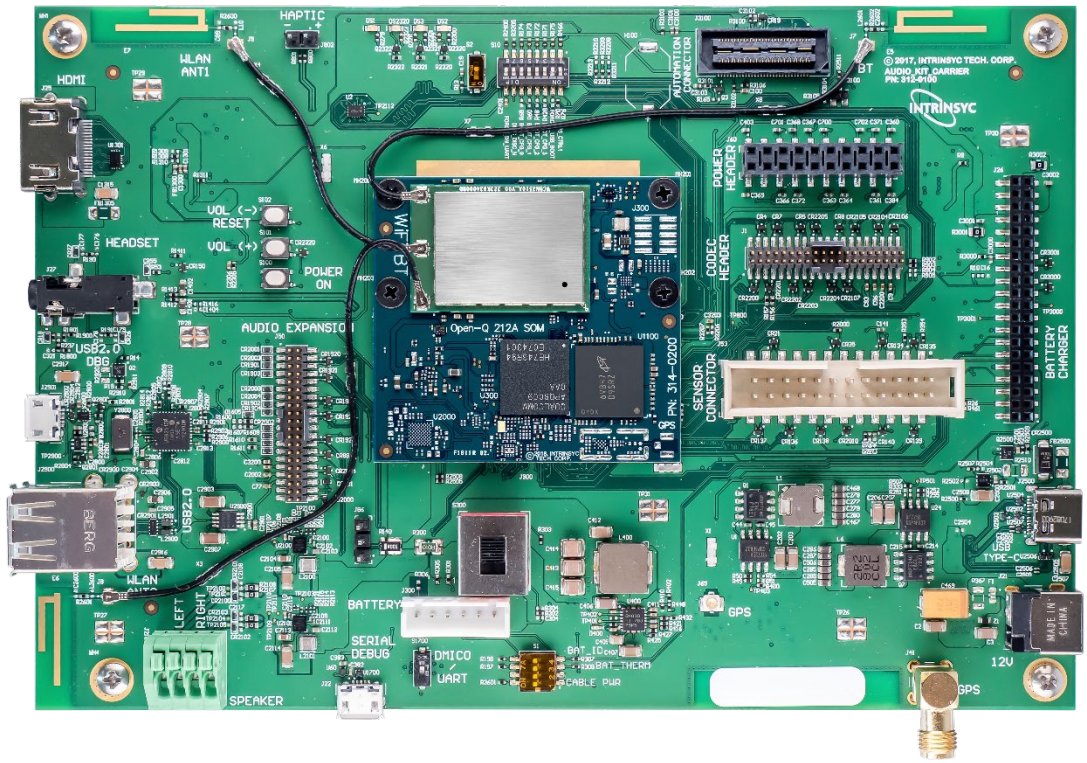

Figure 1 Assembled Open-Q 212A Development Kit

The development kit comes with Linux Home Hub OS software pre-programmed on the SOM. Please contact Lantronix for availability of display adaptors, camera modules, sensor boards, and other accessories: sales@lantronix.com

3.5 Getting Started

This section explains how to setup the Open-Q 212A Development Kit and start using it.

3.5.1 Registration

To register the development kit and gain access to the Lantronix support site, please visit: http://www.intrinsyc.com/resources.

To proceed with registration, the development kit serial number is required. The serial number can be found on the label on the top side of the SOM. The label contains the Serial Number and WIFI MAC address.

Note: Please retain the SOM and carrier board serial number for warranty purposes.

Please visit http://tech.intrinsyc.com/projects/serialnumber/wiki for more details about locating the serial number for registering the development kit.

3.5.2 Powering Up the Development Kit

1. At a static-safe workstation, remove the development kit board carefully from the anti static bag.
2. Connect the serial debug USB (17) to your favorite terminal program if you wish to see boot messages (FTDI UART — USB bridge driver required on PC).
3. Connect the Power Adapter to the 12V DC Jack (11) and then press and hold the POWER ON button (26) for a few seconds until the blue LED starts blinking to indicate the board is booting up.
4. Once the board is booted up you can log into the console with the following username and password:
    - Username: root
    - Password: oelinux123

3.6 Development Kit Block Diagram

The following diagram explains the interconnectivity and peripherals on the Open-Q 212A development platform. Note that not all HW features shown here may be supported by current SW.

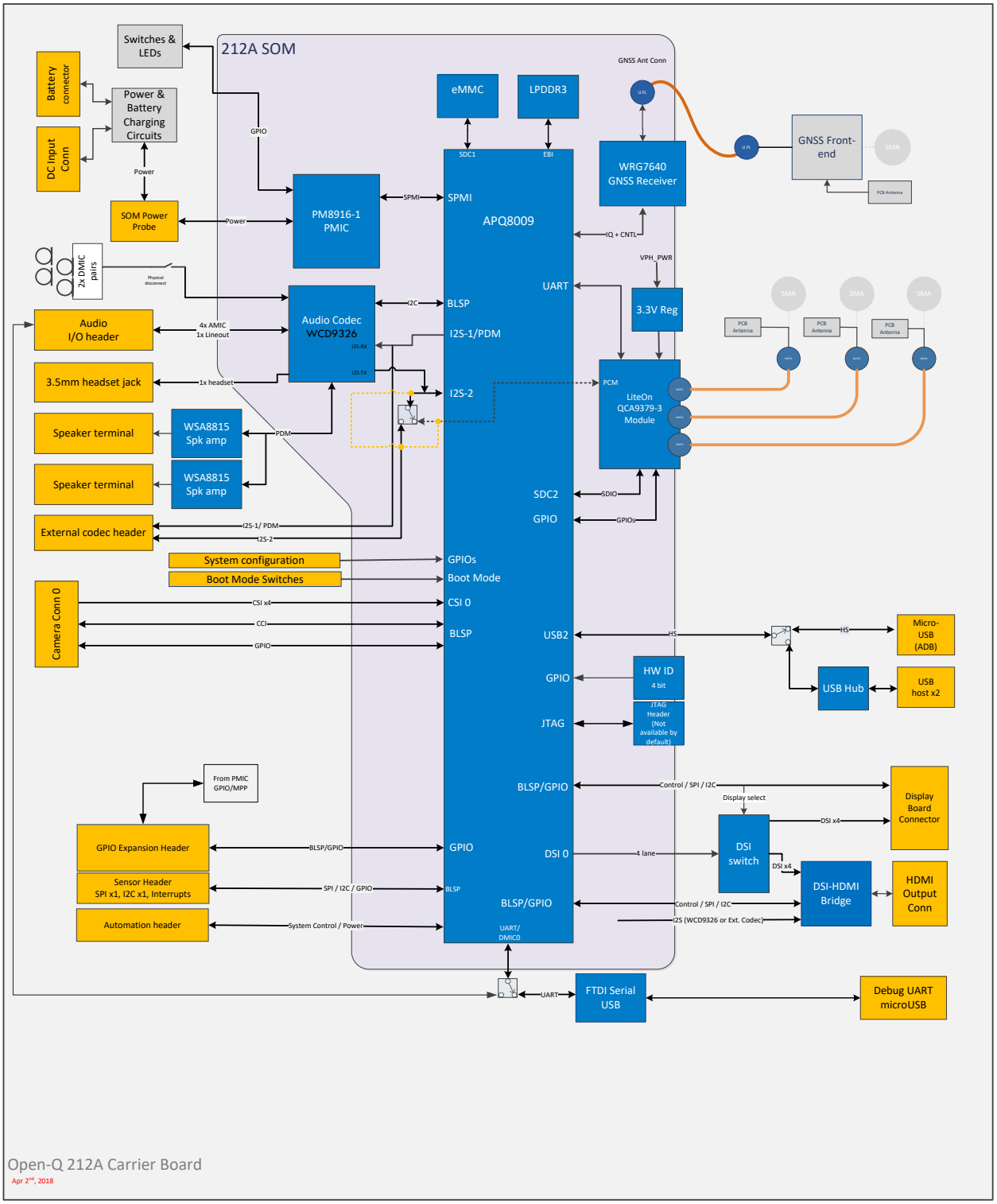

Figure 2 Open-Q 212A Platform Block Diagram

3.7 Open-Q 212A SOM

The Open-Q 212A SOM measuring in 50mm x 46.5mm is where all the processing occurs. It is connected to the carrier via three 100-pins board to board (B2B) connectors.

The SOM provides the basic common set of features with minimal integration efforts for end users.

It contains the following:

- Qualcomm 212 (APQ8009) application processor
- 1GB LPDDR3 RAM
- 4GB eMMC Flash
- PM8916-1 PMIC for Peripheral LDOs, Boost Regulators, Battery Charging
- Pre-certified 802.11a/b/g/n/ac MU-MIMO Wi-Fi/BT Module (with Qualcomm® QCA9379-3)
- Audio Codec (Qualcomm® WCD9326)

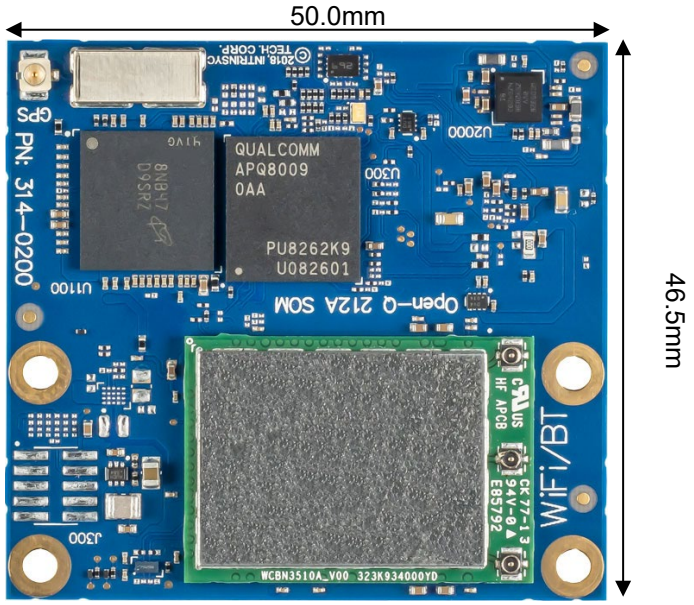

Figure 3 Open-Q 212A SOM

3.7.1 Hardware Features

The Open-Q 212A SOM platform encompasses the following hardware features:

Table 1 Open-Q 212A SOM Features

Feature	Specification
Processor	Qualcomm® 212 (APQ8009) built on 14nm technology • Octa-Core 32-bit ARM Cortex A7 1.3GHz, 512kB L2 cache • Qualcomm® Adreno™ 304 GPU • Qualcomm® QDSP6 DSP

Power Management	Qualcomm® PM8916-1
Memory/Storage	1GB LPDDR3 RAM/ 4GB eMMC Flash
Wireless	Wi-Fi/BT module - 802.11a/b/g/n/ac, 2x2 MU-MIMO, 2.4/5Ghz, Bluetooth 4.2 + BLE (Qualcomm® QCA9379-3) 3x MHF 4 antenna connectors - Two for Wi-Fi, One for Bluetooth
GNSS	Qualcomm® WGR7640 GNSS Receiver
Audio Interfaces	Various audio interfaces with Qualcomm® WCD9326
I/O	2x USB2.0 Type-A host ports, 1x USB micro-b client ADB port, 1x debug UART
OS Support	Linux Home Hub OS
Operating Environment	Power input: 3.6V to 4.2V Operating Temperature: 0°C to +50°C Carrier board connection: 3x 100-pins board-to-board connectors Dimension: 50mm x 46.5mm

3.7.2 SOM RF Interfaces for Wi-Fi and Bluetooth Antennas

The Wi-Fi/BT module on the SOM includes the following RF antenna interfaces:

- ANT0: Wi-Fi antenna 1
- ANT1: Wi-Fi antenna 2
- ANT2: Bluetooth antenna

Wi-Fi antennas: The ANT0 port is for one of the two Wi-Fi antennas and ANT1 is for the other Wi-Fi antenna. Since the Wi-Fi module uses 2x2 MIMO technology and operates in both the 2.4GHz and 5GHz bands, two dual-band antennas are required to be connected to achieve the full performance of the Wi-Fi interface. By default, both antenna ports are connected to the carrier board PCB antennas labelled “WLAN ANT1” and “WLAN ANT2” via coaxial cables. Other suitable antennas may be used by connecting them directly to the Wi-Fi antenna ports on the module with MHF4 coaxial connectors.

Bluetooth antenna: The ANT2 port is for a dedicated Bluetooth antenna. By default, this port is connected to the carrier board PCB antenna labelled “BT” via a coaxial cable.

The Wi-Fi/BT module is designed with a dedicated Bluetooth antenna port so that the Bluetooth and Wi-Fi antennas can be physically separated in the end product to provide better isolation between them. This is done to improve concurrent Wi-Fi and Bluetooth operation. The greater the separation between antennas, the better the concurrent Wi-Fi – Bluetooth performance will be.

For details on how the Wi-Fi module connects to the on-board PCB antennas on the carrier board, refer to section **Error! Reference source not found.**.

3.7.1 SOM RF Interface for GNSS Antenna

The SOM includes one U.FL type coaxial connector for the GNSS receiver antenna, with a +2.7v bias on it to provide power for an active GNSS antenna. By default, this port is connected to the carrier board PCB antenna labelled “GPS” via a coaxial cable. If desired, a suitable GNSS antenna with a U.FL connector could be connected directly to the SOM antenna port by carefully removing the carrier board coaxial cable.

For more information about connecting a GPS antenna to the development kit see section 3.8.15**Error! Reference source not found.** below.

Note that the GNSS receiver may not be supported by all SW versions. Please refer to the latest SW Release Notes document to confirm support.

3.8 Open-Q 212A Carrier Board

The Open-Q™ 212A Carrier board measures 17cm x 11.5cm and has various connectors for different peripherals.

Table 2 Open-Q 212A Carrier Board Features

Feature	Specification
Audio	• 6x Digital Mics via expansion Board • Stereo speaker output • I2S/SLIMBUS interface for external audio devices • 3.5mm audio headset jack
I/O	USB (Micro-b, for ADB), Debug UART interface (via USB micro-b), USB Type-A (x2), GPIO expansion header (GPIO, UART, SPI, I2C buses), Haptics Driver
Wireless antennas	▪ 2x Wi-Fi PCB antennas (2x2 MIMO) + separate Bluetooth PCB antenna for isolation
OS support	Linux Home Hub OS
Power	• 12V DC **(default option)** or • Single-cell Li-ion Battery **(Not supported in BSP Ver 1.0, function will be added in the future BSP)**

The following sections provide details on expansion connectors and switches on the carrier board that allow users to expand the Open-Q™ 212A functionality. Users should ensure the devices they connect to the carrier board meet the specific operating range.

3.8.1 Configuration Dip Switch – S10

DIP switch S10 locates on the top side of the OPEN-Q™ 212A carrier board. This 8-bit switch allows user to config various system functions and boot options. See table below for function of each switch position.

Table 3 Dip Switch HW / SW configuration

Function	DIP Switch	Description	Notes
GPS_CTRL1	S10-1 (A)	GPS Antenna Selection **OFF (Default): On-board PCB Antenna** ON: External Antenna (J41)	See Section 3.8.15
FORCED_USB_BOOT	S10-2 (B)	**OFF (Default): Normal boot** ON: Enables boot from USB function	

Function	DIP Switch	Description	Notes
BOOT_CONFIG[3]	S10-3 (C)	APQ_GPIO_79 / BOOT_CONFIG[3] **OFF (Default): Low** ON: High	Refer to carrier board schematics for boot option
BOOT_CONFIG[2]	S10-4 (D)	APQ_GPIO_78 / BOOT_CONFIG[2] **OFF (Default): Low** ON: High	Refer to carrier board schematics for boot option
BOOT_CONFIG[1]	S10-5 (E)	APQ_GPIO_77 / BOOT_CONFIG[1] **OFF (Default): Low** ON: High	Refer to carrier board schematics for boot option
BOOT_CONFIG[0]	S10-6 (F)	APQ_GPIO_76 / BOOT_CONFIG[0] **OFF (Default): Low, watchdog enabled** ON: High, watchdog disabled	Watchdog
DMIC_DISC_N	S10-7 (G)	DMICs disable **OFF (Default): Disable DMICs** ON: Enable DMICs. See Section 3.8.27	DMICs privacy control
FORCE_SW_UART	S10-8 (H)	Debug Console UART selection **OFF (Default): Debug console selected** ON: Enable DMICs. See Section 3.8.27	Connects USB cable to J22 on carrier board to use debug console

3.8.2 12V DC Jack – J21

The development kit can be powered by connecting the bundled 12V DC power supply to the power supply jack, J21, on the carrier board. The development kit is configured to be powered by the 12V DC by default. Please refer to Section 3.8.3 and Section 3.8.6 for power source configuration setting.

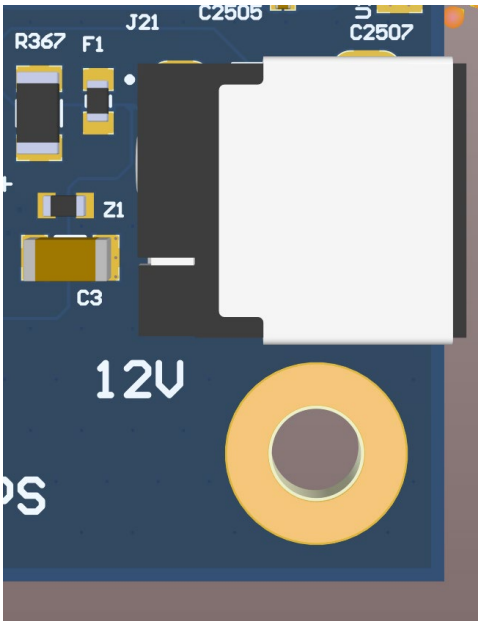

Figure 4 12V DC Power Jack (J21)

3.8.3 SOM Power Source Selection Switch – S300

Switch S300 allows the user to power the SOM using either the 12V DC power supply or a Lithium battery. See table below for selecting the correct power source for the SOM.

Table 4 Power Source Selection

Switch location	Up (Illustrated in figure below)	Down
SOM power source	12V DC	Battery (through battery connector J300)

Note 1: The 12V DC still needs to be plugged in should user needs the following power rails to power any device on the carrier board:

- MB_VREG_5P0
- MB_VREG_3P3
- MB_VREG_1P8
- VREG_5P0_HDMI
- MB_ELDO_CAM0_DVDD

- MB_ELDO_CAM1_DVDD
- MB_ELDO_CAM1_VCM

Note 2: See Section 3.8.4 and Section 3.8.5 for setting up the development kit to be powered by a battery

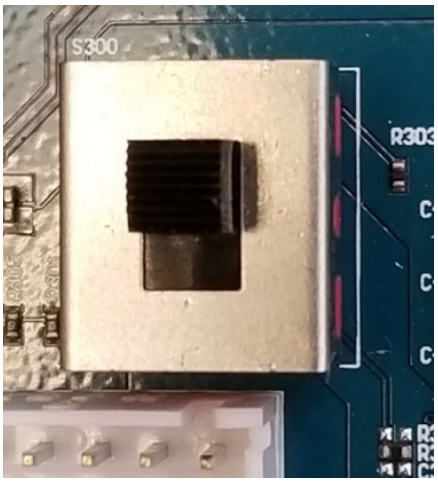

Figure 5 SOM Power Source Switch (S300), Up position shown

3.8.4 Battery Connector – J300

J300 allows user to connect a single-cell rechargeable Lithium battery pack to power the development kit.

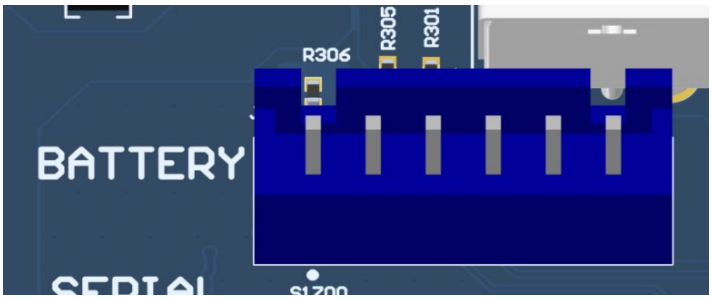

Figure 6 Battery Connector (J300)

Table 5 Battery Connector (J300) Specification

Manufacturer	JST	
Part Number	B6B-XH-A(LF)(SN)	
Mating connector	XHP-6	Manufactured by JST

Nominal Battery Voltage	3.7V	
Max. Battery Voltage	4.2V	
Battery ID	Support	See Section 3.8.5 for more information
Thermistor	Support (10k Expected)	See Section 3.8.5 for more information

Table 6 Battery Connector (J300) Pinout

Description	Signal	Pin #
GND	GND	1
		2
Connection to Battery Thermistor. 10K thermistor expected.	BATT_THERM_CONN	3
Connection to Battery ID Pin	BATT_ID_CONN	4
Battery Positive Voltage connection	VBATT_CONN	5
		6

3.8.5 Battery Dip Switch – S1

This 4-bit switch allows the user to control the battery configuration and boot options. Table 7 below outlines the pinout and connections of this DIP switch.

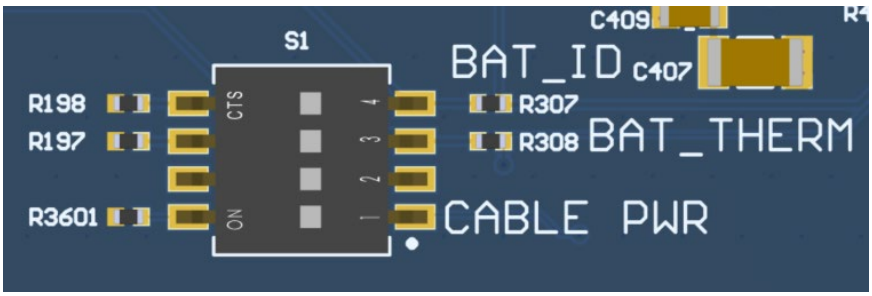

Figure 7 Battery Dip Switch (S1)

Table 7 Battery DIP Switch S1 configuration

Function	Switch Position	Description	Notes
CBL_PWR_N	1	Auto boot Selection **ON (Default): System will auto boot whenever power is applied** OFF: User needs to press the power button to turn on the system after power is applied	
NC	2	No Function	
BAT_THERM	3	Battery Thermistor **ON (Default): Uses the 10k resistor (R197) on the carrier board to simulate battery thermistor presents** OFF: Use battery's thermistor	Set this switch to ON when using a battery that does not have a built-in thermistor.
BAT_ID	4	Battery ID **ON (Default): Uses the 51k resistor (R198) on the carrier board to simulate battery ID presents** OFF: Use battery's ID	Set this switch to ON when using a battery and the battery does not have an ID pin.

3.8.6 External Battery-Charger Header – J26

The External Battery-Charger Header exposes battery charging related signals for an external battery charger. Please refer to the schematic to disable the SOM battery-charger before using this header. The pinout of this header is descripted in below.

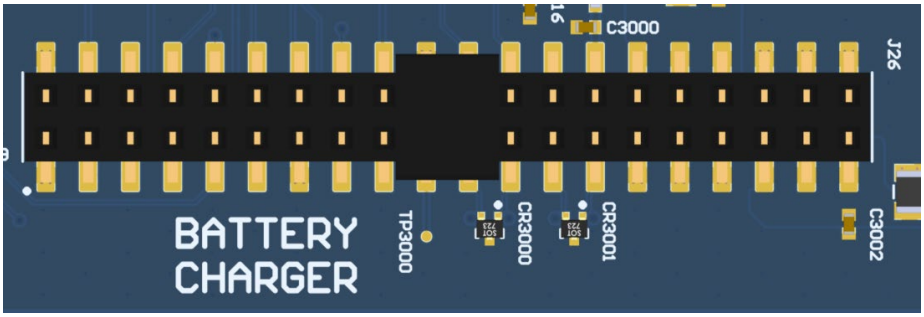

Figure 8 External Battery-Charger Header (J26)

Table 8 External Battery Charger Header J26 Pinout

Description	Signal	Pin #	Pin #	Signal	Description
GND	GND	1	2	GND	GND
Battery Positive Voltage Sense	BATT_P	3	4	PMI_VDD_CAP	Not available on 212A
Battery Negative Voltage Sense	BATT_N	5	6	CHG_VBAT_SNS	Not available on 212A
Battery ID Pin	BAT_ID	7	8	PMI_CHG_EN	Not available on 212A
Battery Thermistor Pin	BAT_THERM	9	10	SMB_PARALLEL_CHG_EN	APQ GPIO_66 Default: SMB_EN on external charger for parallel charging
PM8916-1 VREF_BAT_THM	PM_VREF_BATT_THERM	11	12	SMB_INT	APQ GPIO_95
GND	GND	13	14	SMB_STAT_N	APQ GPIO_71
Not available on 212A	PMI_GPIO_1	15	16	FG_ALARM	APQ GPIO_17
NC	NC	17	18	BATT_CHG_EXP_TP2	NC
No connection on Carrier Board	BATT_CHG_EXP_TP1	19	20	GND	GND
APQ GPIO_5 BLSP2 Bit 2 Default: UART2_RX *Switch S10-8 must be set to OFF.	GPIO_5_BLSPx_UART_RX	21	22	OPT_1	PM8916-1 OPT_1 Leave Unconnected
APQ GPIO_4 BLSP2 Bit 3 Default: UART2_TX *Switch S10-8 must be set to OFF.	GPIO_4_BLSPx_UART_TX	23	24	OPT_2	PM8916-1 OPT_2 Leave Unconnected

Description	Signal	Pin #	Pin #	Signal	Description
APQ GPIO_7 BLSP2 Bit 0 Default: I2C2_SCL	GPIO_7_BLSPx_I2C_SCL	25	26	NC	NC
APQ GPIO_6 BLSP2 Bit 1 Default: I2C2_SDA	GPIO_6_BLSPx_I2C_SDA	27	28	BATT_EXP_1P8	+1.8V output (VREG_L5_1P8)
GND	GND	29	30	BATT_EXP_SYS_PWR	SOM_SYS_PWR_PER (SOM Power Input)
GND	GND	31	32		
GND	GND	33	34		
USB_VBUS for SOM and USB Ports (J2901) on Carrier Board	BATT_EXP_USB_VBUS	35	36	GND	GND
		37	38	GND	GND
		39	40	GND	GND

3.8.7 Power Probe Header – J86

J86 allows user to measure the power consumed by the SOM during operation. User can measure the voltage across the 0.005Ω sense resistor (R140) and calculate the current consumed. Pinout of J86 is provided in below.

Figure 9 J86 Power Probe Header

Table 9 Power Header J86 Pin out

Pin #	Description	Signal
1	SOM power positive current sense line	SOM_PWR_SENSE_P
2	SOM power negative current sense line	SOM_PWR_SENSE_N

Pin #	Description	Signal
3	GND	GND

3.8.8 Power Header – J60

The Power Header allows user to power their peripherals from the carrier board. Please see the pinout below for voltage level.

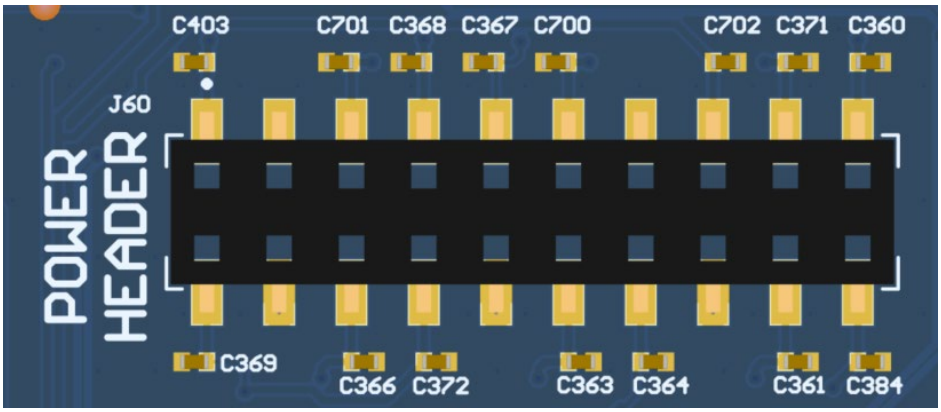

Figure 10 Power Connector (J60)

Table 10 Power Header J60 Pinout

Description	Signal	Pin #	Pin #	Signal	Description
PM8916-1 VREG_L17	VREG_L17_2P85	2	1	MB_ELDO_CAM0_DVDD	CAM0 1V1 DVDD LDO (U5)
GND	GND	4	3	NC	NC
3V3 Rail LDO (U24) output	MB_VREG_3P3	6	5	VREG_L4_1P8	PMI8916-1 VREG_L4
PM8916-1 VREG_L17	VREG_L17_2P85	8	7	MB_ELDO_CAM1_DVDD	CAM1 1V1 DVDD LDO (U6)

Description	Signal	Pin #	Pin #	Signal	Description
GND	GND	10	9	MB_ELDO_CAM1_VCM	CAM1 VCM LDO (U10) output
3V3 Rail	MB_VREG_3P3	12	11	VREG_L4_1P8	PMI8916-1 VREG_L4
PMI8916-1 VREG_L10	VREG_L10_2P85	14	13	NC	NC
GND	GND	16	15	VREG_L11_SDC	PMI8916-1 VREG_L11
3V3 Rail	MB_VREG_3P3	18	17	VREG_L4_1P8	PMI8916-1 VREG_L4
12V from J300	DC_IN_12V	20	19	MB_VREG_5P0	5V LDO (U1) output

3.8.9 Debug Serial UART – J22

The UART debug console can be accessed via J22 (USB micro-b). The UART signals are translated to USB signal by the FTDI FT232RQ chip on the carrier board. Please ensure the FTDI virtual COM port driver has been installed on your PC. **Note**: This port provides access to the APQ UART interface only, for ADB function, please use J2901. See Section 3.8.24.

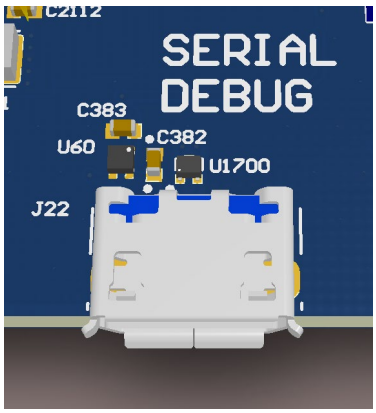

Figure 11 J22 Debug UART over USB

The following DIP Switch needs to be set in order to use the UART:

DIP Switch S10 Position 8 'FORCE_SW_UART' = OFF/OPEN

Serial Port Settings:

Baud Rate: 115200

Data: 8 bits

Parity: None

Stop:1 bit

Flow Control: None

3.8.10 Sensor IO Expansion Header – J53

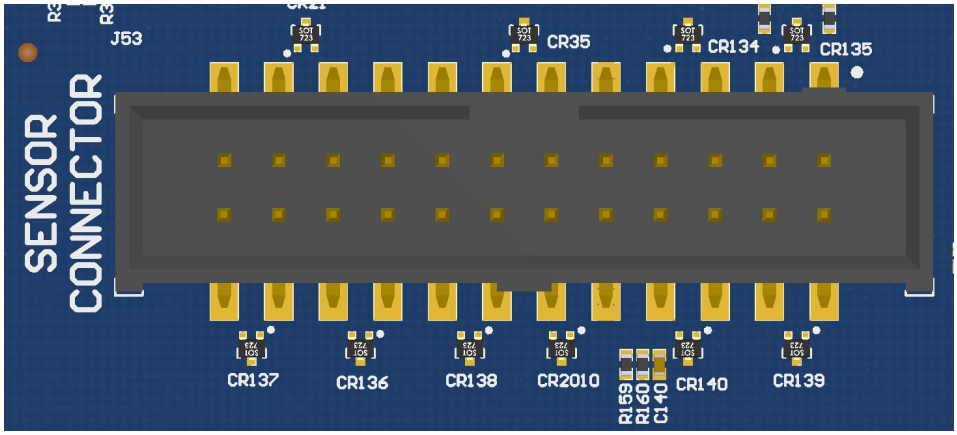

Figure 12 J53 Sensor Expansion Header

The sensor expansion header (J53) allows user to connect to an optional home automation connectivity accessory board that features the Qualcomm QCA4024 Zigbee/BLE chip. Users can also use this port to connect their own peripherals. Various low-speed buses are available on this header. Please refer to the schematic and check power draw before connecting peripheral to this header.

Table 11 Sensor Expansion Header (J53) Pinout

Description	Signal	Pin #	Pin #	Signal	Description
Accelerometer interrupt input (APQ GPIO_96)	SENSOR_ACCEL_INT	2	1	GPIO_6_BLSPx_I2C_SDA	Sensor I2C SDA (APQ GPIO_6)
Interrupt input (APQ GPIO_65)	SENSOR_CAP_INT_N	4	3	GPIO_7_BLSPx_I2C_SCL	Sensor I2C SCL (APQ GPIO_7)
Gyroscope interrupt input (APQ GPIO_36) *Not available by default. See SOM SCH	SENSOR_GYRO_INT	6	5	GPIO_XX_SENSOR_RST	Sensor reset signal output (APQ GPIO_67)
Sensor Analog power supply (VREG_L10_3P0)	SENS_ANA_PWR	8	7	VREG_L6_1P8	Sensor IO PWR 1.8 V VREG_L6_1P8
GND	GND	10	9	GND	GND
Touch screen interrupt input (APQ GPIO_13)	TS_INT_N	12	11	SENSOR_HRM_INT	HRM interrupt input (APQ GPIO_110)
Alternate sensor interrupt input (APQ GPIO_94)	SENSOR_ALSP_INT_N	14	13	GPIO_48_SPI6_CS1_MAG_N	Magnetic Switch Interrupt input (APQ GPIO_97)
Digital Compass interrupt input (APQ GPIO_50) *Not available by default. See SOM SCH	SENSOR_MAG_DRDY_INT	16	15	NC	NC
Pressure Sensor interrupt input (APQ GPIO_12. *Shared with PWR_SRC_DET	GPIO_XX_PRESSURE_INT	18	17	NC	NC
Sensor SPI MOSI (APQ GPIO_8)	BLSP6_3_SPI_MOSI	20	19	BLSP6_1_SPI_CS_N	Sensor SPI Chip Select (APQ GPIO_10)
Sensor SPI MISO (APQ GPIO_9)	BLSP6_2_SPI_MISO	22	21	BLSP6_0_SPI_CLK	Sensor SPI CLK (APQ GPIO_11)
APQ GPIO_38	CCI_TIMER2	24	23	NC	NC

3.8.11 Headset Audio Jack – J27

J27 is a standard 3.5mm TRRS jack in CTIA pinout order with headset detection support. Signals are routed to Audio CODEC WCD9326 on the SOM. This function is not supported in BSP V1.0 and maybe supported in the future BSP.

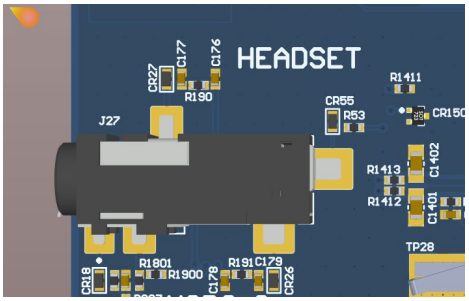

Figure 13 Audio Headset Jack (J27)

3.8.12 Audio Input Expansion Header – J50

J50 allows the user to easily access all audio input related signals from the Audio CODEC (QCOM WCD9326) on the SOM.

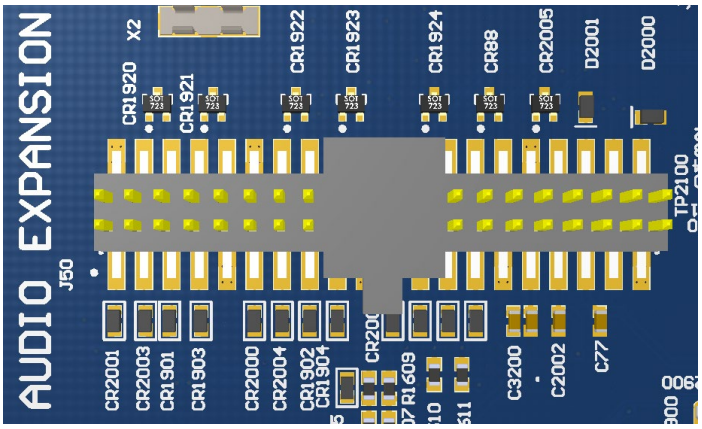

Figure 14 Audio Input Expansion Header (J50)

Table 12 Audio Input Expansion Header (J50) Pinout

Note	Signal	Pin #	Pin #	Signal	Note
	CDC_MIC1_P	1	2	GND	
	CDC_MIC1_N	3	4	624_DMIC0_CLK	See Section 3.8.27
	CDC_MIC2_P	5	6	624_DMIC0_DATA	See Section 3.8.27
	CDC_MIC2_N	7	8	CDC_DMIC1_CLK	
	GND	9	10	CDC_DMIC1_DATA	
	CDC_MIC3_P	11	12	GND	
	CDC_MIC3_N	13	14	CDC_DMIC2_CLK	
	CDC_MIC4_P	15	16	CDC_DMIC2_DATA	
	CDC_MIC4_N	17	18	CDC_DMIC3_CLK	Not Available on the 212A dev. kit
	GND	19	20	CDC_DMIC3_DATA	Not Available on the 212A dev. kit
	CDC_MIC_BIAS 1	21	22	GND	
	CDC_MIC_BIAS 2	23	24	PMI_GPIO_1	Not Available on the 212A dev. kit
	CDC_MIC_BIAS 3	25	26	212_DMIC0_CLK	APQ GPIO_5
Not Available on the 212A dev. kit	CDC_MIC_BIAS 4	27	28	212_DMIC0_DATA	APQ GPIO_4
	GND	29	30	GPIO_MIC_MUTE_STATUS	APQ GPIO_92

Note	Signal	Pin #	Pin #	Signal	Note
PM8916-1	VREG_L5_1P8	31	32	GND	
U24 on Carrier Board	MB_VREG_3P3	33	34	GPIO_XX_MIC_SELECT	APQ GPIO_51
U1 on Carrier Board	MB_VREG_5P0	35	36	CDC_LINE_OUT_3	
	NC	37	38	CDC_LINE_OUT_REF	
	GND	39	40	CDC_LINE_OUT_4	

3.8.13 External Codec/GPIO Expansion Header – J1

J1 allows user to access SLIMBUS, I2S, power rails, and other GPIOs from APQ or PM8916-1 that are not used by another peripheral on the carrier board. Please refer to the pinout table below for detail.

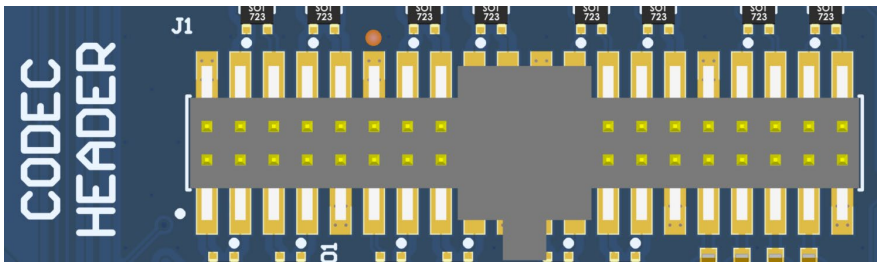

Figure 15 External Codec/GPIO Expansion Header (J1)

Table 13 External Codec/GPIO Expansion Header J1 Pinout

Description	Signal	Pin #	Pin #	Signal	Description
Not Available on the 212A dev. kit	GPIO_0_BLSP1_SPI_MOSI	1	2	GND	GND
Not Available on the 212A dev. kit	GPIO_1_BLSP1_SPI_MISO	3	4	PM_GPIO_x_DIV_CLK2	PM8916-1 GPIO_2
BLSP1 bit 1 (APQ GPIO 14)	GPIO_2_BLSP1_SPI_CS_N	5	6	PM_MPP_3	PM8916-1 Multi-Purpose Pin 3

Description	Signal	Pin #	Pin #	Signal	Description
BLSP1 bit 0 (APQ GPIO 15)	GPIO_3_BLSP1_SPI_CLK	7	8	MI2S_1_D3	Not Available on the 212A dev. kit Can be configured as APQ GPIO_93 by installing R2111 on CB
GND	GND	9	10	MI2S_1_D2	Not Available on the 212A dev. kit Can be configured as APQ GPIO_93 by installing R2122 on CB
APQ GPIO 98	WCD_INT	11	12	GND	GND
Not Available on the 212A dev. kit	B2B_SLIMBUS_DATA1	13	14	MI2S_1_D1	MI2S Bus 1 – Data bit 1 (APQ GPIO_63)
Not Available on the 212A dev. kit	B2B_SLIMBUS_DATA0	15	16	MI2S_1_D0	MI2S Bus 1 – Data bit 0 (APQ GPIO_62)
Not Available on the 212A dev. kit	B2B_SLIMBUS_CLK	17	18	MI2S_1_WS	MI2S Bus 1 – WS (APQ GPIO_61)
GND	GND	19	20	MI2S_1_SCK	MI2S Bus 1 – SCK (APQ GPIO_60)
Not Available on the 212A dev. kit	MI2S_2_D1_HDR	21	22	GND	GND
Not Available on the 212A dev. kit	MI2S_2_D0_HDR	23	24	GPIO_96_OR_53	APQ GPIO_**53**
Not Available on the 212A dev. kit	MI2S_2_WS_HDR	25	26	GPIO_98_OR_55	APQ GPIO_**55**
Not Available on the 212A dev. kit	MI2S_2_SCK_HDR	27	28	GPIO_68_AMP_PWR_EN	APQ GPIO_**72**
GND	GND	29	30	GPIO_25_MI2S_MCLK	Primary MI2S master clock A (APQ GPIO_25)

Description	Signal	Pin #	Pin #	Signal	Description
	VREG_L5_1P8	31	32	GND	GND
U24 on Carrier Board	MB_VREG_3P3	33	34	212_GPIO_75	General Purpose. GPIO 75
U1 on Carrier Board	MB_VREG_5P0	35	36	212_GPIO_84	General Purpose. GPIO 84
Main 12V DC	DC_IN_12V	37	38	GPIO_45_AMP_FAULT	General Purpose. APQ GPIO **36**
GND	GND	39	40	GPIO_44_AMP_RST_N	General Purpose. APQ GPIO **50**

3.8.14 On Board PCB WLAN and BT Antennas

The Open-Q™ 212A carrier board has two on board WLAN PCB antennas and one on board Bluetooth Antenna that connects to the QCA9379 Wi-Fi module on the SOM via MHF 4 coaxial cables. These antennas connect to the SOM in the following configuration:

Table 14 Wi-Fi and Bluetooth Antennas Connectors

Antenna (on carrier)	Connector (on carrier)	Connector (QCA9379 Wi-Fi Module on SOM)
WLAN ANT1 (E7)	J9	ANT0
WLAN ANT2 (E6)	J8	ANT1
BT ANT (E5)	J7	BT

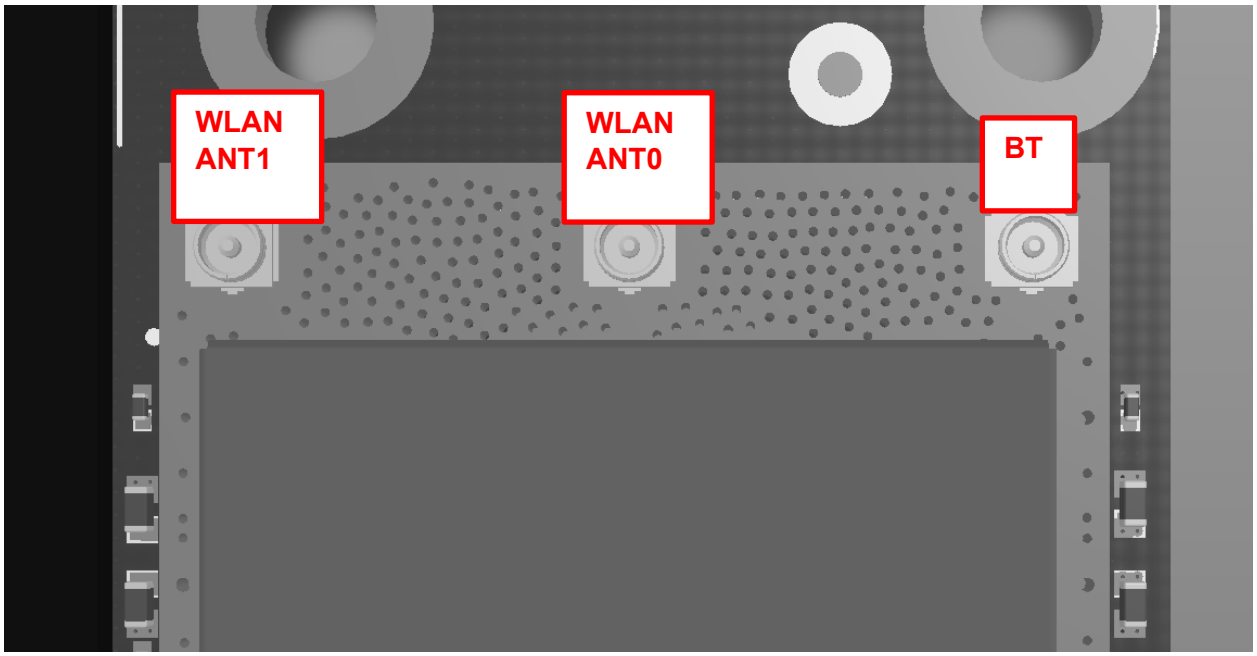

Figure 16 WLAN Module Antenna Connections

3.8.15 GNSS PCB Antenna and External Antenna Connections

The Open-Q 212A SOM supports GNSS function by using the Qualcomm WGR7640 GNSS Receiver. User can select either the PCB antenna on the carrier board (E4) or the external antenna connection (J41) to receive GNSS signal by toggling S10 position 1.

Table 15 GPS/GNSS Antenna Selection

S10 position 1	Antenna Selection
OFF (Default)	**On-board PCB Antenna (E4)**
ON	External Antenna (connects user antenna to J41)

Note that the GNSS receiver may not be supported by all versions of SW. Please check with the latest SW Release Notes document to confirm support.

3.8.16 HDMI Connector – J25

J25 is a standard HDMI connector. Note that the HDMI output may not be supported by all versions of SW. Please check with the latest SW Release Notes document to confirm support.

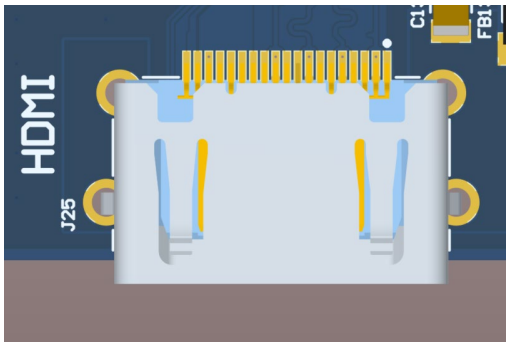

Figure 17 HDMI Connector (J25)

3.8.17 Display Connector – J2

J2 allows user to connect the development kit to a MIPI DSI display. Note that the MIPI DSI output may not be supported by all versions of SW. Please check with the latest SW Release Notes document to confirm support.

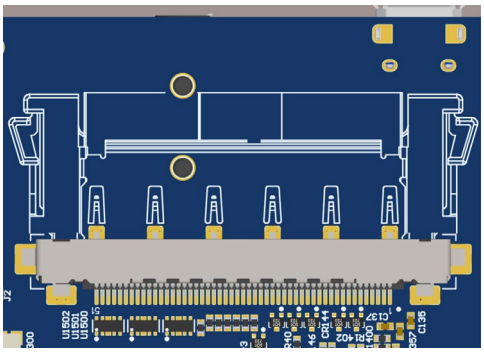

Figure 18 Display Connector (J2)

3.8.18 Camera Connector – J5

J5 allows the Open-Q 212A development kit to connect to a MIPI CSI camera module. Pinout of this connector are given below. Please note that only the J5 camera port is supported on the Open-Q 212A platform.

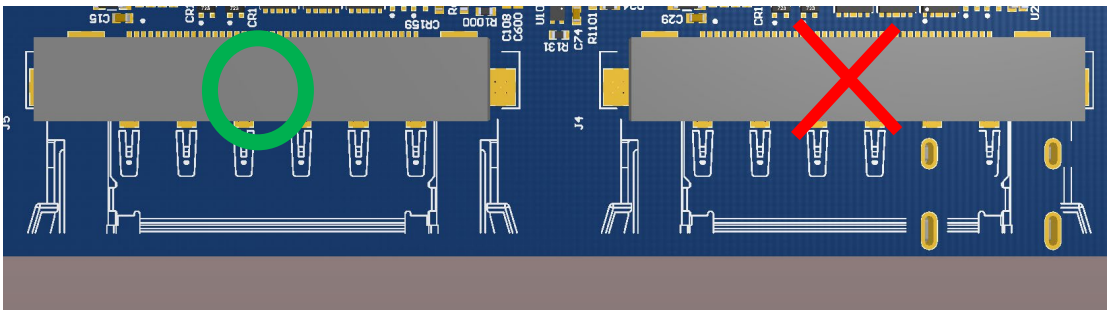

Figure 19 Camera Connectors (J5 – left, J4 – right)

Table 16 Camera Connectors (J5, J4) Pin Out

Pin	Signal	Note
1	CSI0_EXT1_PWR	MB_VREG_3P3
2	CSI0_EXT1_PWR	
3	CSI0_EXT1_PWR	
4	GND	
5	CSI0_AVDD	VREG_L17_2P85
6	CSI0_DVDD	VREG_L2_1P1
7	CSI0_ACT_VDD	VREG_L10_2P85
8	CSI0_ACT_VDD	
9	CSI0_DOVDD	VREG_L6_1P8
10	CSI0_DOVDD	
11	CAM_MUTE_CONN0_GND	
12	CAM0_FLASH_EN	
13	CAM1_RST_N	
14	CAM1_STANDBY_N	
15	GPIO_30_CCI_I2C_SCL0	
16	GPIO_29_CCI_I2C_SDA0	
17	CAM_MCLK0	
18	CAM0_FLASH_TRIG	
19	GND	
20	MIPI_CSI0_LANE0_N	
21	MIPI_CSI0_LANE0_P	
22	GND	
23	MIPI_CSI0_CLK_N	
24	MIPI_CSI0_CLK_P	

Pin	Signal	Note
25	GND	
26	MIPI_CSI0_LANE1_N	
27	MIPI_CSI0_LANE1_P	
28	GND	
29	MIPI_CSI0_LANE2_N	
30	MIPI_CSI0_LANE2_P	
31	GND	
32	MIPI_CSI0_LANE3_P	This pair's order is swapped intentionally
33	MIPI_CSI0_LANE3_N	
34	GND	
35	GPIO_31_CCI_I2C_SDA1	
36	GPIO_32_CCI_I2C_SCL1	
37	CAM0_IRQ	
38	CAM0_MCLK3	Not available
39	CSI0_DVDD	
40	CAM0_EXT_PWR	MB_VREG_5P0. Not available by default
41	CAM0_EXT_PWR	

3.8.19 Automation Connector Header – J3100

J3100 is used for automating tests on the development platform and is not supported by Lantronix for customer use. This header contains certain power rails and system control signals that users can access should they need to. ***If this connector is to be used, remove R300 and disable battery source using switch S300 (see Section 3.8.3). Please refer to carrier and SOM schematics for more details.**

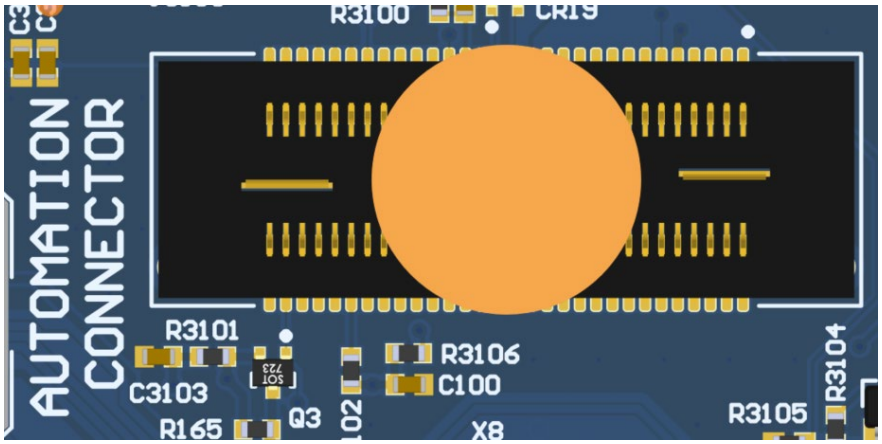

Figure 20 J3100 Automation connector header

Table 17 Automation Connector J3100 Pin Out

Pin #	Signal	Description
9	VREG_MDM_1P8	VREG_L5_1P8
11	APQ_PS_HOLD	Power supply hold signal output from APQ to
27	USB_VBUS_DISBL	Input used to disconnect VBUS from USB Ports.
29	KYPD_PWR_N	Power Button input
31	RESIN_N	Reset Button input
35	AUTO_12V	DC_IN_12V
37	PM_PON_RESET_N	Reset output from PMIC
47	FORCED_USB_BOOT	Input. High to enter FORCED USB BOOT mode
49, 51, 53, 55, 57, 59	AUTO_VBATT	Input. +3.9V System Power for SOM.
50	PLATFORM_ID	Connected to VREG_L5_1P8
58	APQ_RESOUT_N	Reset output from APQ

*** Only connected pins are listed.**

3.8.20 Haptic Motor Header – J802

This two-pins header is intended to be connected to a haptic vibration motor. It is a programmable voltage output that is referenced to VPH_PWR. This feature is not supported in BSP V1.0.

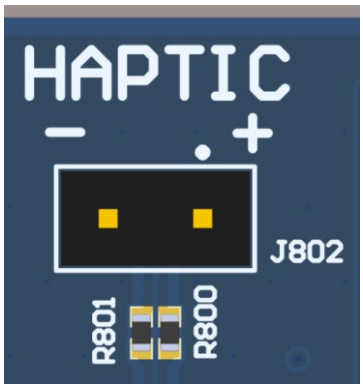

Figure 21 Haptic Motor Header (J802)

Table 18 Haptic Motor Header Pinout (J802)

Pin #	Signal
1	HAP_OUT_P (VPH_PWR)
2	HAP_OUT_N (VIB_DRV_N from PM8916-1)

3.8.21 Buttons – S100, S101, S102

There are three push-buttons (S100, S101, and S102) on the carrier board to allow users to interact with the system. Note that the buttons may not all be supported by all versions of SW. Please check with the latest SW Release Notes document to confirm support.

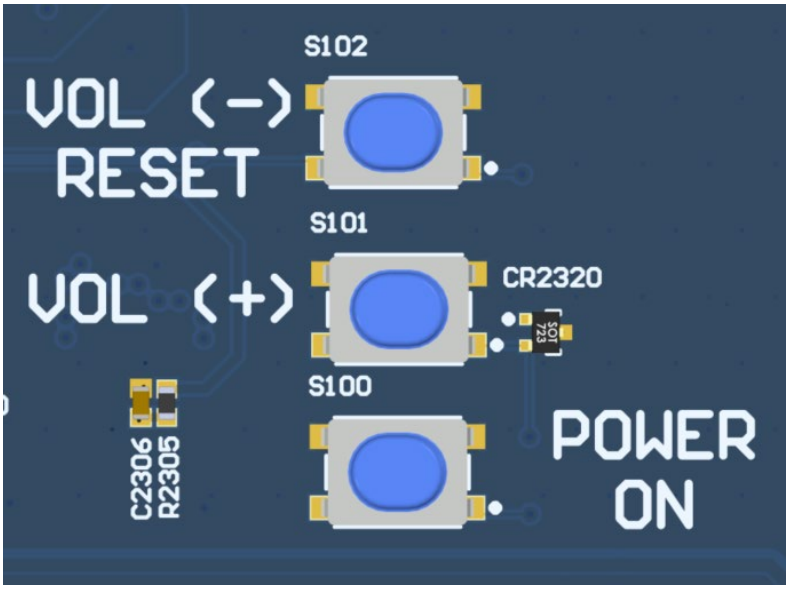

Figure 22 Buttons (S100, S101, S102)

Table 19 Buttons Function description (S100, S101, S102)

Buttons	Function	Description
S100	Power Button	System Power On, Standby
S101	Volume Up	Increase volume
S102	Volume Down / Reset	Decrease volume, hold to reset system (FW dependent)

3.8.22 LED Indicators – DS1, DS2, DS3, DS2320

There are four LEDs on the carrier board for indication purpose. Please refer to the table in below for their respective functions.

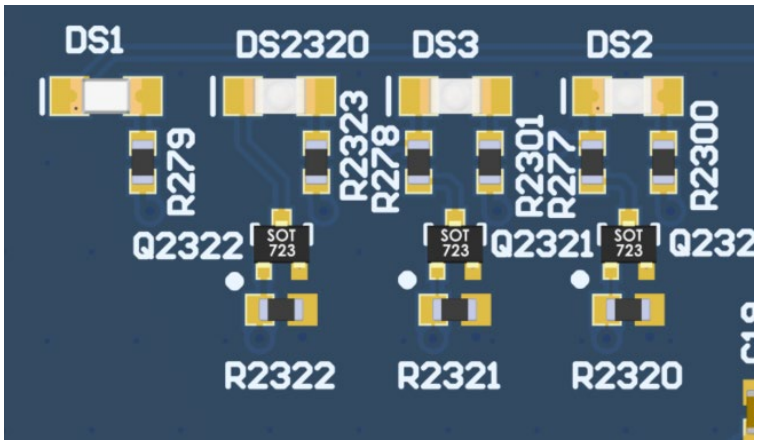

Figure 23 Indicator LEDs (DS1, DS2, DS3, DS2320)

Table 20 Indicator LEDs (DS1, DS2, DS3, DS2320)

LED	Colour	Function
DS1	Red	PM8916-1 CHD_LED for charging indication
DS2	Blue	APQ GPIO_69 for general purpose *PMIC MPP control is not available on the 212 Audio Kit
DS3	Green	APQ GPIO_68 for general purpose *PMIC MPP control is not available on the 212 Audio Kit

LED	Colour	Function
DS2320	Green	USB_HUB_ACTIVE from U2800 (USB Hub IC) to indicates hub is active

3.8.23 USB Type C Port – J2500

J2500 is standard USB 3.0 Type-C connector. This connector has no function on the 212A Development Kit.

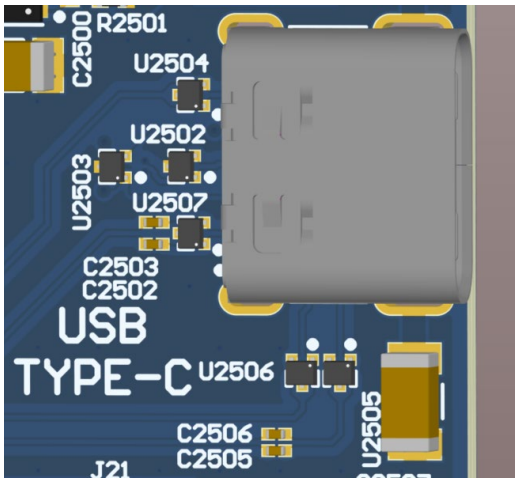

Figure 24 USB Type C Port J2500

3.8.24 USB Micro-B Connector – J2901

J2901 is a standard USB Micro-B connector allowing the 212A development kit to act as a device or ADB device when connected to a PC.

Note: This connector connects to the USB PHY of on the SOM and is different than J22 listed in Section 3.8.9 on the carrier board.

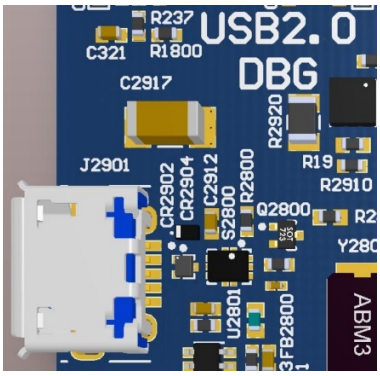

Figure 25 USB Micro-B Connector (J2901)

3.8.25 USB 2.0 Type-A Ports – J2900

There are two ports USB 2.0 Type-A ports provided by the USB switch hub IC (U2800). These ports follow the industry standard and have a maximum current output of 500mA on each port.

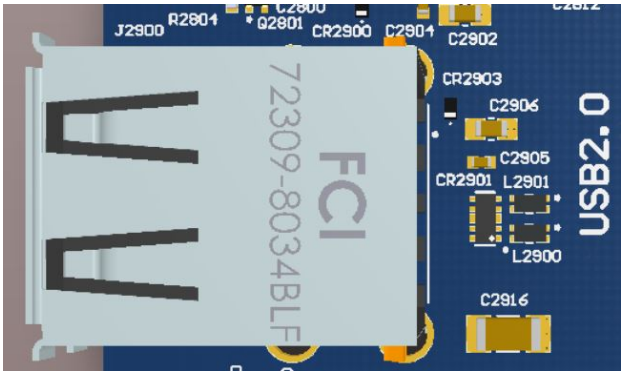

Figure 26 USB Micro B Connector (J2900)

3.8.26 WSA8815 Speaker Amplifiers Out – J2100

J2100 allows users to connect to two speakers in stereo configuration. These outputs are driven by the WSA8815 Audio AMP. on the carrier board and the WCD9326 Audio CODEC on the 212A SOM.

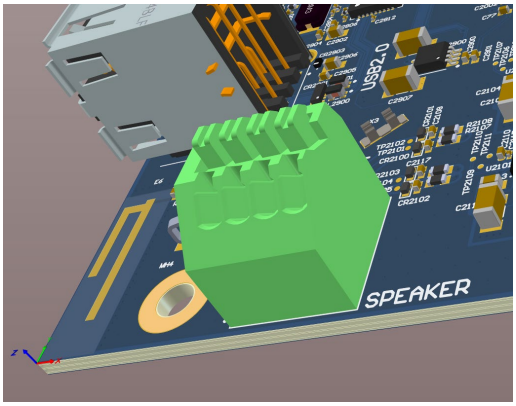

Figure 27 4-position wire to board terminal (J2100)

Table 21 WSA8815 Speaker AMP Out Connector (J2100)

Pin #	Signal	Description
1	WSA_SPKR_L_N	Left Speaker Negative
2	WSA_SPKR_L_P	Left Speaker Positive
3	WSA_SPKR_R_N	Right Speaker Negative
4	WSA_SPKR_R_P	Right Speaker Positive

3.8.27 DMICs

There are three pairs of DMICs on the carrier for audio recording. Please configure dip switches on the carrier board as listed below to enable them.

Table 22 DMICs details

DMIC	Signal	Power Source	Instruction
U1601/U1602	CDC_DMIC1_CLK_SW/ CDC_DMIC1_DATA_SW	CDC_MIC_BIAS1	Set Switch S10 position 7 to ON (Closed)
U1603/U1604	CDC_DMIC2_CLK_SW/ CDC_DMIC2_DATA_SW	CDC_MIC_BIAS3	Set Switch S10 position 7 to ON (Closed)
U1609/U1610	624_212_DMIC0_CLK_SW/ 624_212_DMIC0_DATA_SW	CDC_MIC_BIAS1	1. Set Switch S10 position 7 to ON (Closed) 2. Set Switch S10 position 8 to ON (Closed) 3. Set Switch S1700 to ON (Closed)
U1605/U1606	**Not Supported on 212A Development kit**		

3.8.28 DMIC/UART DEMUX Switch – S1700

S1700 controls the DMIC and UART path. See Section 3.8.27.

3.9 Accessories

3.9.1 Camera Module Accessory

A camera module is available as an optional accessory from the Lantronix online store in the Accessories section: https://shop.intrinsyc.com/

The compatible camera accessory is based on the 5MP OmniVision OV5640 sensor with YUV output and interfaces to the development kit through the included 21cm JAE interface cable to connector J5 on the development kit.

Figure 28 - OV5640 Camera Module