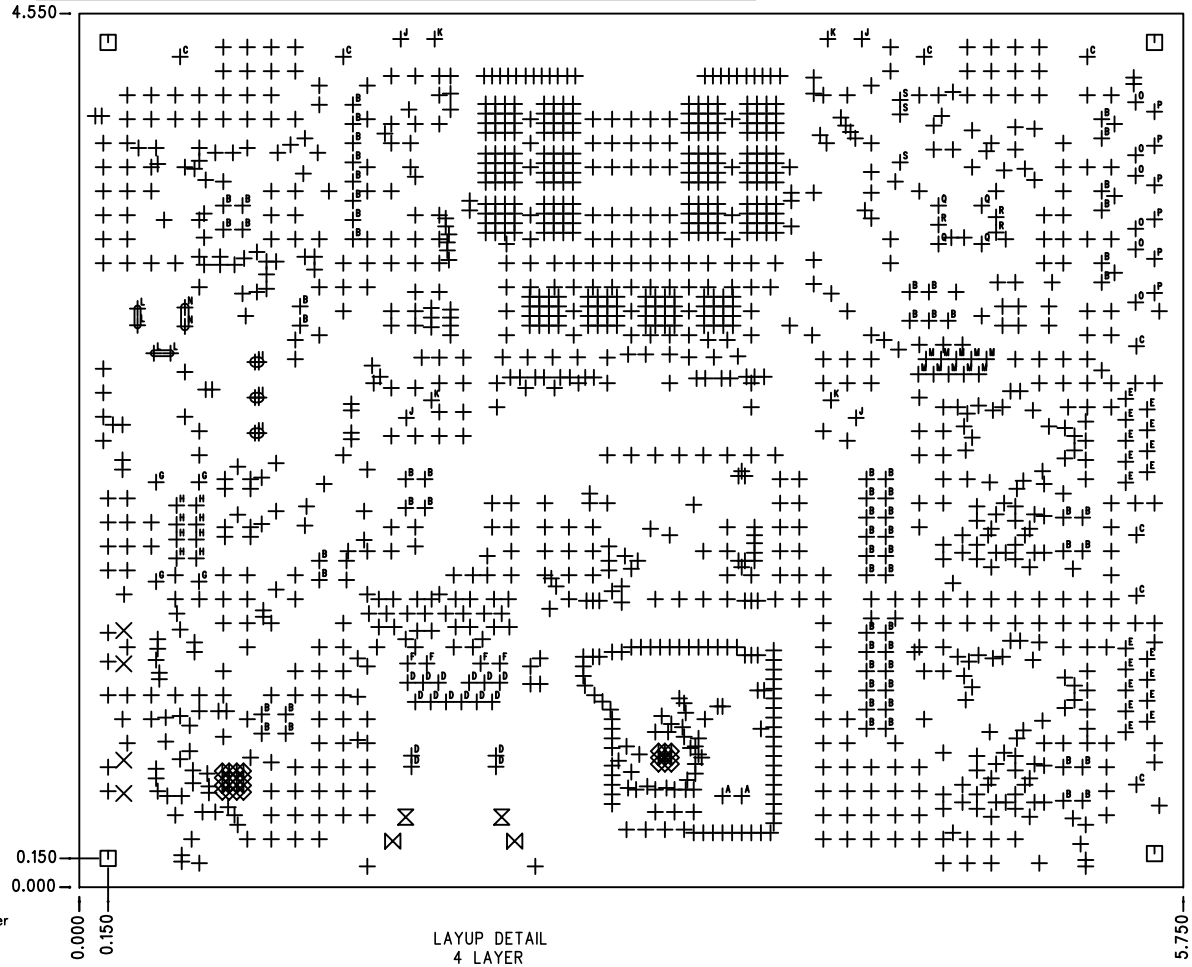
IMPEDANCE CONTROLLED SIGNALS

Signal & Pairs	Trace Width	Impedance Requirement	Signal Layers	Reference Layer
ETHx+/ETHx− ETX_ETHx+/ETX_ETHx−	8.2 MIL TRACE 11.8 MIL GAP	100 Ohm +/−10% differential 50 Ohm+/−10% single−ended	Layer 4	Layer 3
DDP/DDM HDPx/HDMx HFSDPC/HFSDMC HHSDPx/HHSDMC SDDP/SDDM	8.1 MIL TRACE 7.9 MIL GAP	90 Ohm +/−10% differential	Layers 1&4	Layers 2&3
All others	8 MIL	50 Ohm +/−10% single−ended	Layers 1&4	Layers 2&3

REVISION HISTORY

A	Initial Release		
B	−		
C	−		

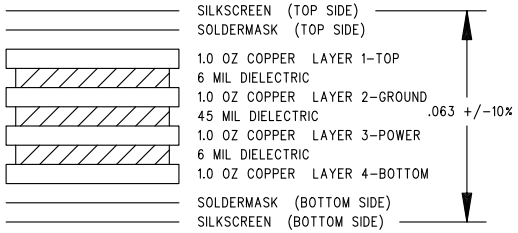
SIZE	QTY	SYM	PLATED	TOL
0.01	1294	+	YES	+/−0.002
0.0101	25	◇	YES	+/−0.003 NOTE 16
0.015	3	S	YES	+/−0.003
0.028	10	M	YES	+/−0.003
0.0315 x 0.11811	2	L	YES	+/−0.003
0.035	16	D	YES	+/−0.002
0.03543	4	X	NO	+0.003/−0.000
0.03622	8	H	YES	+/−0.003
0.037	2	A	YES	+/−0.003
0.039	3	R	NO	+/−0.003
0.03937 x 0.1378	1	N	YES	+/−0.003
0.04	67	B	YES	+/−0.003
0.041	6	P	YES	+/−0.002
0.045	4	F	YES	+/−0.003
0.047	18	E	YES	+/−0.003
0.05 x 0.07	3	I	YES	+/−0.003
0.053	6	O	YES	+/−0.002
0.062	2	⋈	YES	+/−0.003
0.06299	4	K	NO	+/−0.003
0.09055	4	G	YES	+/−0.003
0.094	4	Q	NO	+/−0.003
0.09606	4	J	NO	+/−0.003
0.125	8	C	YES	+/−0.005
0.128	2	⧖	NO	+/−0.005
0.175	4	□	YES	+/−0.005



Notes: apply unless specified otherwise.

1. Material: Polyclad PCL−FR−370HR or equivalent. Overall thickness = .063+/−10%
2. Unless otherwise specified, all hole dimensions apply after plating. All plated through holes to have a minimum of .001" copper.
3. All holes shall be located within .003" diameter of true position. Layer to layer registration shall be within .003". All holes surrounded by land shall have a minimum annular ring of .001". All .010 via in pads must be filled with THP−100DX1 material.
4. Apply LPI (liquid photo imageable) soldermask over bare copper. Soldermask to be per IPC−SM−840, type B, class 3. Color: ORANGE.
5. All exposed copper shall be coated with electroless nickel/immersion gold finish. Nickel plating shall be 118−275u" thick over copper. Gold plating shall be 2−8u" thick over nickel. Boards shall pass solderability testing per J−STD−003. There shall be no evidence of exposed copper.
6. Warp or twist of board shall not exceed .010 inch per inch.
7. Silkscreen using non−conductive epoxy ink. Color: WHITE.
8. Remove all burrs and break all sharp edges.
9. Board shall meet the requirements of UL796 with a flammability rating of 94V−0. Vendor's UL logo or designation shall be located on the solder side of board.
10. Fabricate in accordance with ANSI/IPC−A−600, class 2.
11. Dimensions and tolerances per ASME Y14.5M.
12. Fabricate using artwork 330−306−GBR Rev C
13. Any rework shall be to IPC−R−700C guidelines and tested per section VI. Test results shall be included with each shipment. Reworked items shall be separated from non−reworked items and the outer packaging labeled as "reworked items enclosed".
14. Tent all unplugged vias both sides.
15. All materials and processes must be RoHS compliant.
16. Plug and fill 0.0101 vias with non−conductive material.

LAYUP DETAIL
4 LAYER



Lantronix

TITLE:
FABRICATION DRAWING
Golden Gate Eval Board

DWG	DWG NO:	REV:
A	330−306−FAB−R	C
SIZE	SCALE: 1 : 1	SHEET: 1 OF 1