USB and Ethernet Impedence Requirements

Type	Signal or Diff Signal Pair	Value	Reference to
USB	HHSDMA/HHSDPA HHSDMB/HHSDPB HFSDMC/HFSDPC HDMA/HDPA, HDMB/HDPB HDMC/HDPC, SDDM/SDDP DDM/DDP	90 ohm Differential	Pair-differential
Ethernet	E0TX+/E0TX-, E0RX+/E0RX-, E0TXP/E0TXM, E0RXP/E0RXM	100 ohm Differential 50 ohm Single	Pair-differential Ground-single

REV	HISTORY OF CHANGES	ENGINEER	DATE
A	Initial Schematic of Golden Gate Evaluation Board	M Simonsen	10/2014
B	Updates from first proto build	M Simonsen	5/2015
C	Add power switch, power LED, and incorporate rev E Module footprint	M Simonsen	1/2016

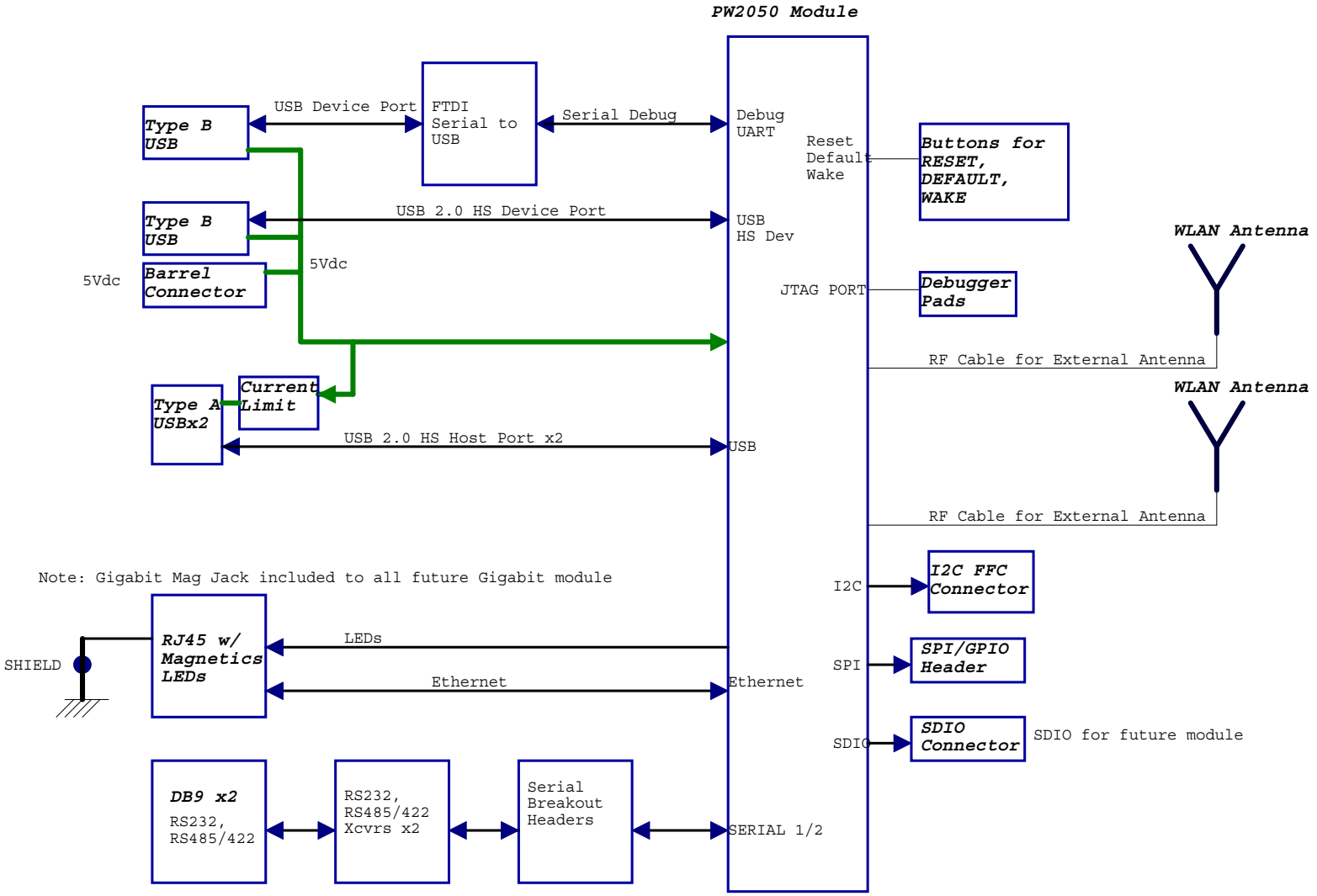
LANTRONIX M Simonsen

Title: PW2050 Eval

Size: C | Document Number: SCH-330-306 | Rev: C

Date: Friday, January 22, 2016 | Sheet 1 of 6

PW2050 Evaluation Board

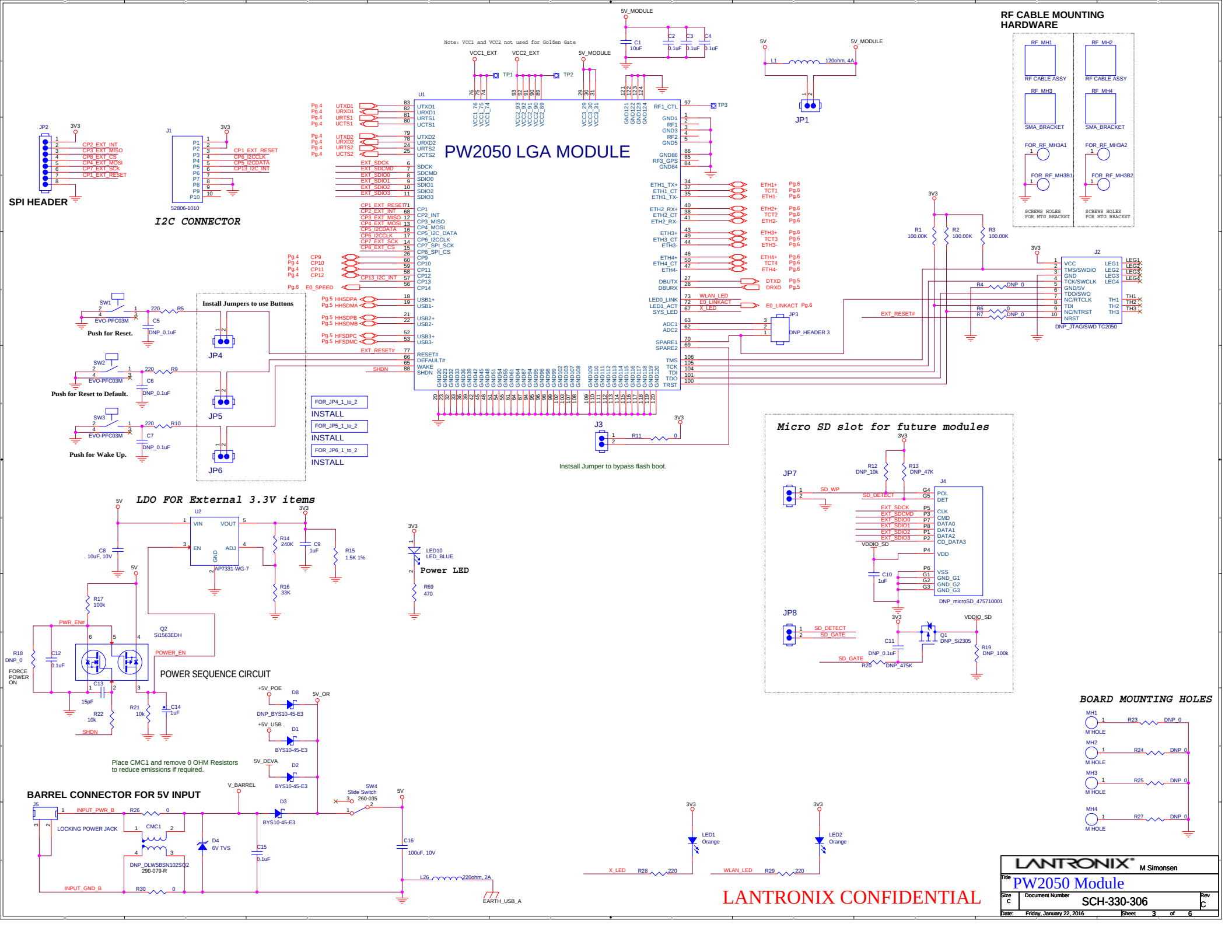


LANTRONIX M Simonsen

Title: BLOCK DIAGRAM

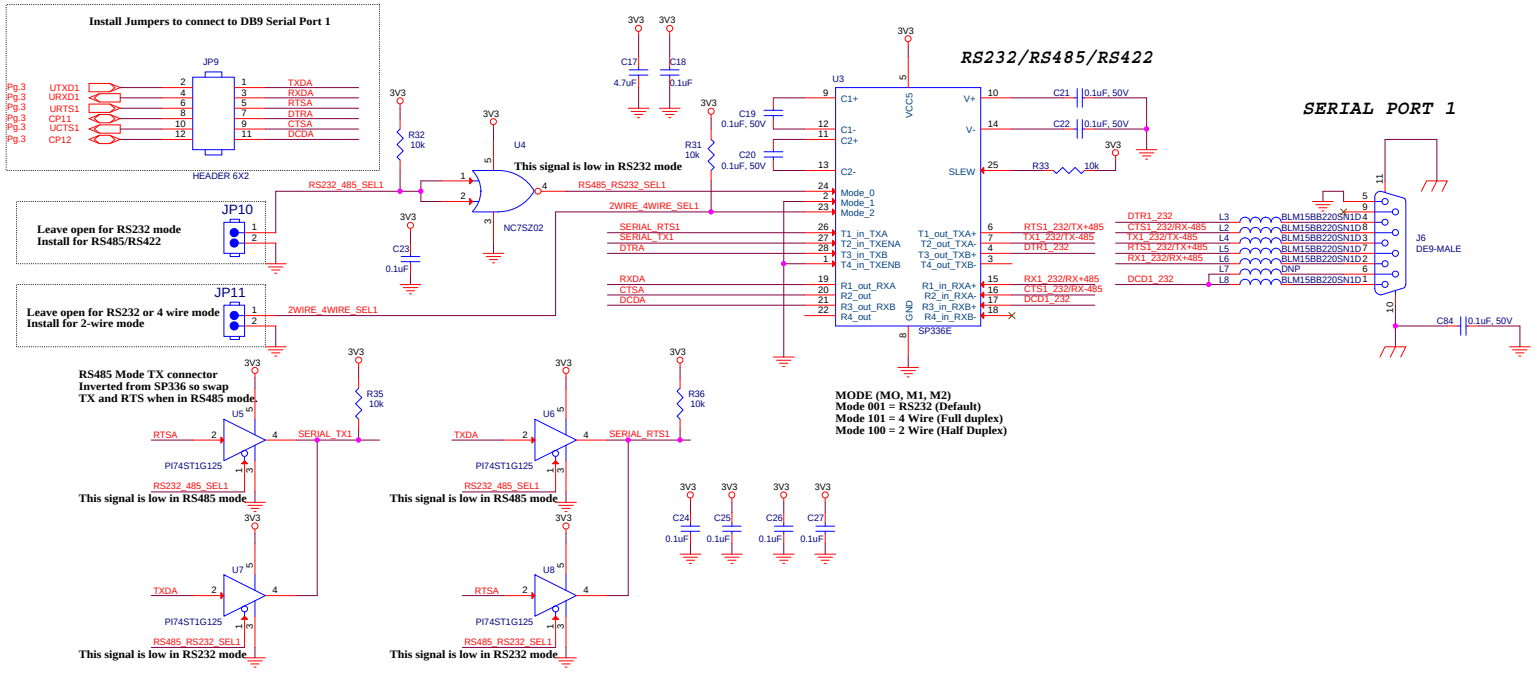
Size: C | Document Number: SCH-330-306 | Rev: C

Date: Friday, January 22, 2016 | Sheet 2 of 6


PW2050 LGA MODULE
SPI HEADER
I2C CONNECTOR
Install Jumpers to use Buttons
Push for Reset.
Push for Reset to Default.
Push for Wake Up.
Instsall Jumper to bypass flash boot.
RF CABLE MOUNTING HARDWARE
Micro SD slot for future modules
LDO FOR External 3.3V items
POWER SEQUENCE CIRCUIT
Power LED
Place CMC1 and remove 0 OHM Resistors to reduce emissions if required.
BARREL CONNECTOR FOR 5V INPUT
BOARD MOUNTING HOLES
LANTRONIX CONFIDENTIAL
M Simonsen
PW2050 Module
SCH-330-306
Friday, January 22, 2016

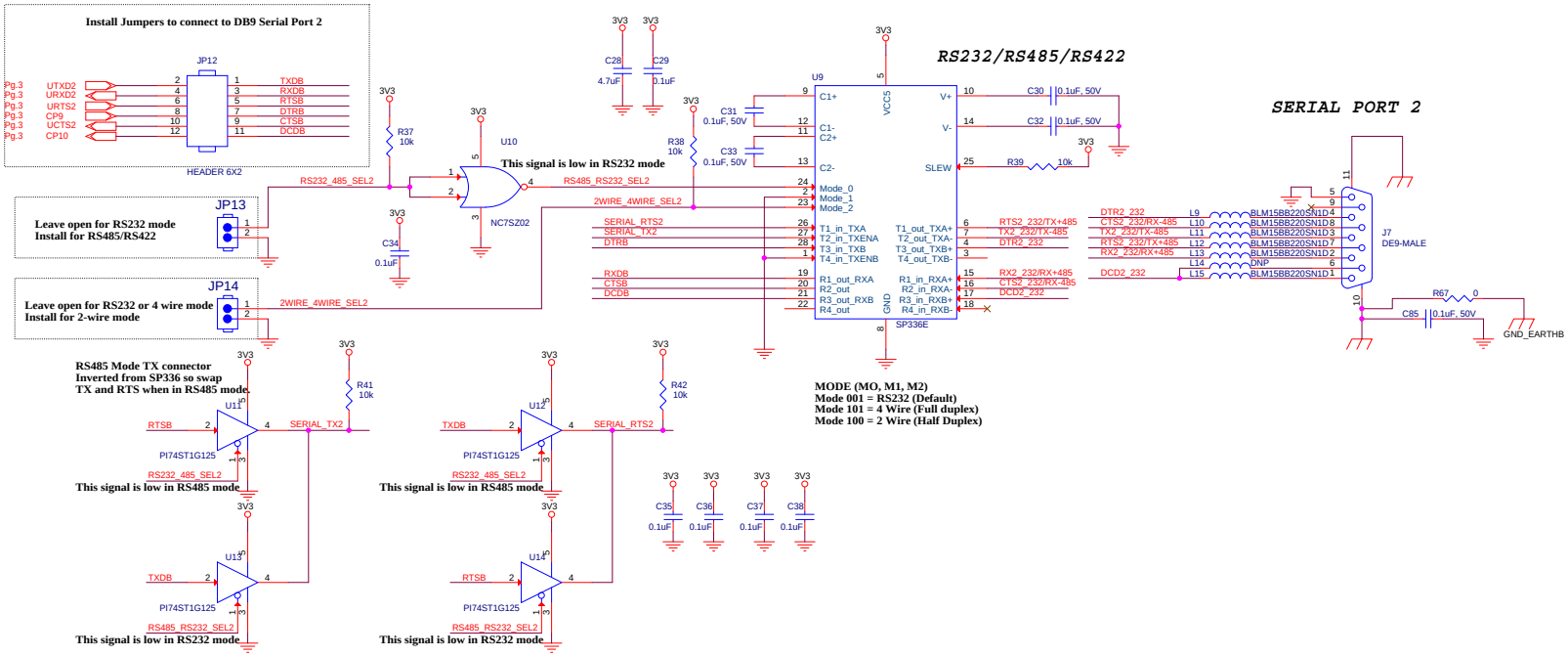
FOR_JP9_1_to_2
INSTALL
FOR_JP9_3_to_4
INSTALL
FOR_JP9_5_to_6
INSTALL
FOR_JP9_7_to_8
INSTALL
FOR_JP9_9_to_10
INSTALL
FOR_JP9_11_to_12
INSTALL

FOR_JP10_hang_1
INSTALL
FOR_JP11_hang_1
INSTALL



FOR_JP12_1_to_2
INSTALL
FOR_JP12_3_to_4
INSTALL
FOR_JP12_5_to_6
INSTALL
FOR_JP12_7_to_8
INSTALL
FOR_JP12_9_to_10
INSTALL
FOR_JP12_11_to_12
INSTALL

FOR_JP13_hang_1
INSTALL
FOR_JP14_hang_1
INSTALL



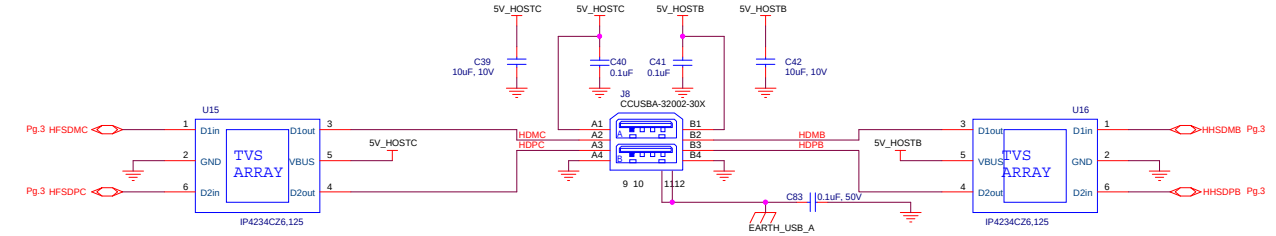
LANTRONIX MSimonsen

Title: Serial Ports 1 and 2

Size: C | Document Number: SCH-330-306 | Rev: C

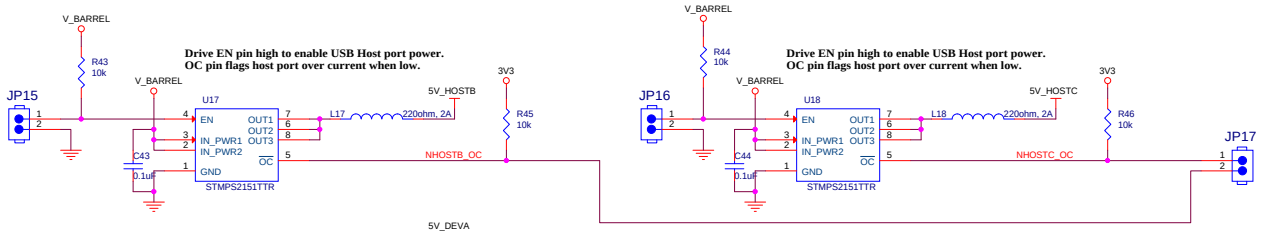
Date: Friday, January 22, 2016 | Sheet 4 of 6

USB HOST INTERFACE

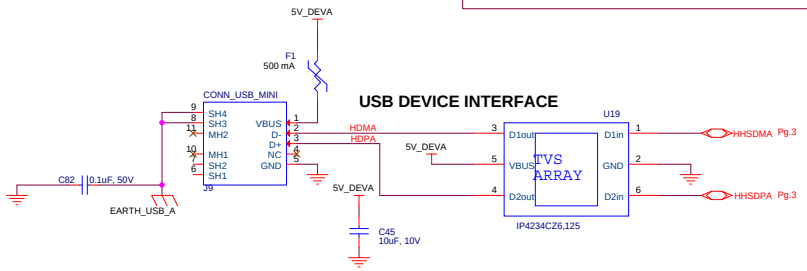


Route the HDPx/HDMx/DDx pairs as 90 ohm differential nets on a layer next to the ground plane. Minimize the use of Vias and keep clear of other nets.

Route the HDPx/HDMx/DDx pairs as 90 ohm differential nets on a layer next to the ground plane. Minimize the use of Vias and keep clear of other nets.

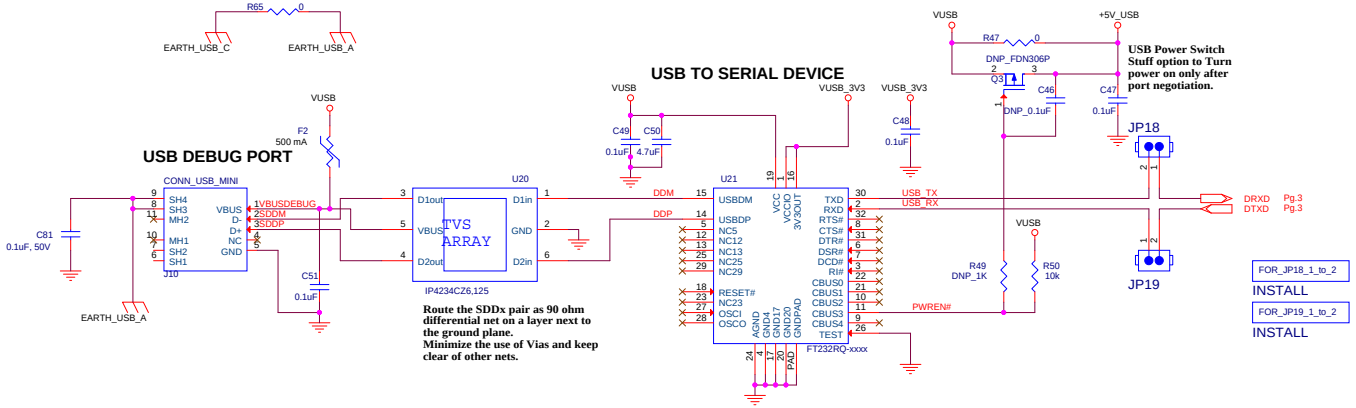


USB DEVICE INTERFACE



Route the HDPx/HDMx/DDx pairs as 90 ohm differential nets on a layer next to the ground plane. Minimize the use of Vias and keep clear of other nets.

USB TO SERIAL DEVICE

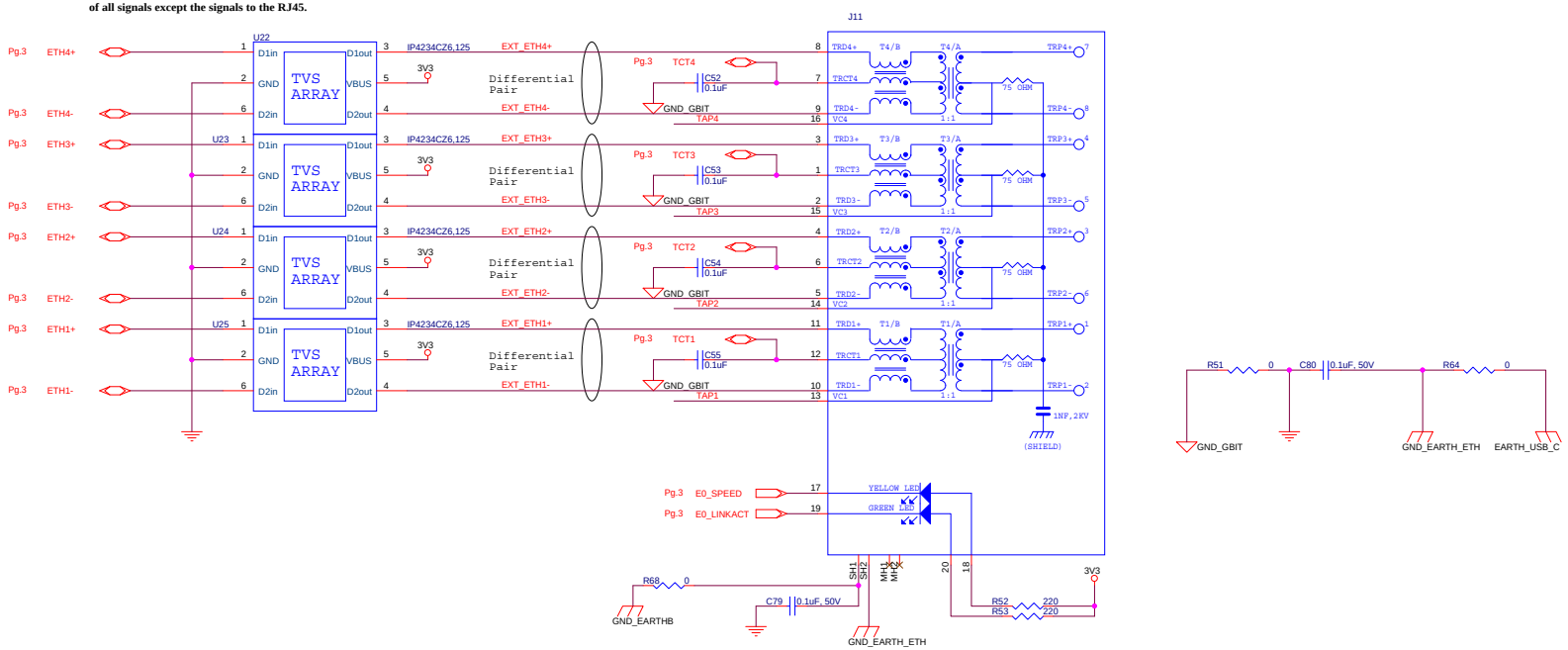


LANTRONIX	M Simonsen	
Title: USB/ IO board connector		
Size: C	Document Number: SCH-330-306	Rev: C
Date: Friday, January 22, 2016	Sheet 5 of 6	

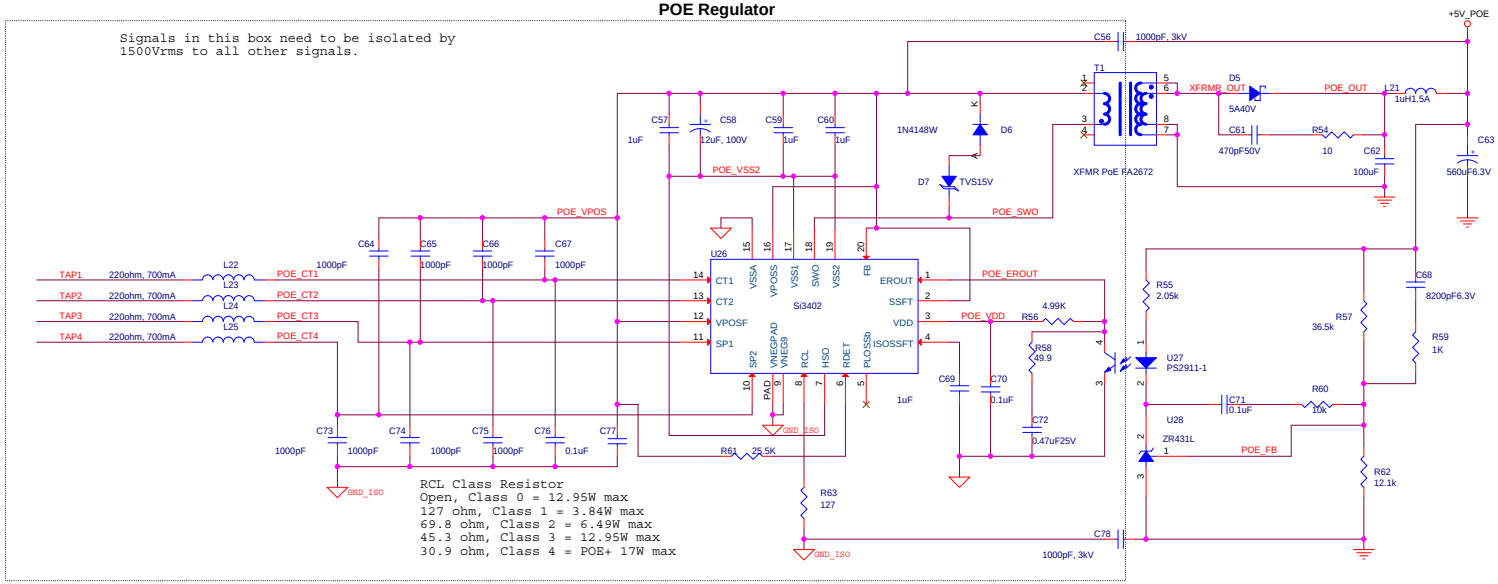
Route the ETHx+/ETHx- pairs as 100 ohm differential nets on a layer next to the ground plane. Minimize the use of Vias and keep clear of other nets. Use 20 mil trace on TCTx. Void area under RJ Jack of all signals except the signals to the RJ45.

ETHERNET POE MAG JACK

Gigabit Mag Jack used for compatibility with future Gigabit modules



POE Regulator



LANTRONIX	M Simonsen	
Title: Ethernet		
Size: C	Document Number: SCH-330-306	Rev: C
Date: Friday, January 22, 2016	Sheet 6 of 6	